AMPEX

AUDIO-VIDEO
SYSTEMS DIVISION

VPR-2 SERIES

TIME-CODE READER/GENERATOR PWA ACCESSORY

OPERATION AND MAINTENANCE

CATALOG NO. 1809449-03
ISSUED: APRIL 1981

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AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

Prepared by

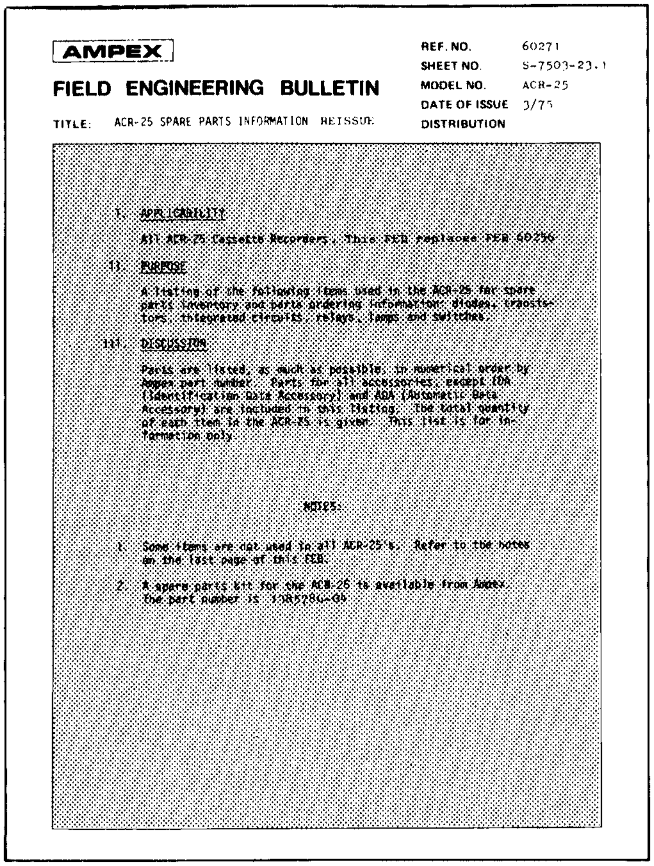
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FIELD ENGINEERING BULLETIN SERVICE


AMPEX

FIELD ENGINEERING BULLETIN

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MODEL NO. ACR-25
DATE OF ISSUE 3/75
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TITLE: ACR-25 SPARE PARTS INFORMATION REISSUE

I. APPLICABILITY

All ACR-25 Cassette Recorders. This FEB replaces FEB 60256

II. PURPOSE

A listing of the following items used in the ACR-25 for spare parts inventory and parts ordering information: diodes, transistors, integrated circuits, relays, lamps and switches.

III. DISCUSSION

Parts are listed, as much as possible, in numerical order by Ampex part number. Parts for all accessories, except IDA (Identification Data Accessory) and ADA (Automatic Data Accessory) are included in this listing. The total quantity of each item in the ACR-25 is given. This list is for information only.

NOTES:

1. Some items are not used in all ACR-25's. Refer to the notes on the last page of this FEB.
2. A spare parts kit for the ACR-25 is available from Ampex. The part number is 1385786-04

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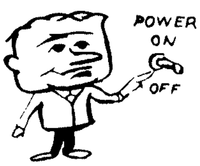
AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION
401 BROADWAY
REDWOOD CITY, CALIFORNIA 94063
(415) 367-2011

Effective: 1 October 1980

SAFETY AND FIRST AID SUGGESTIONS

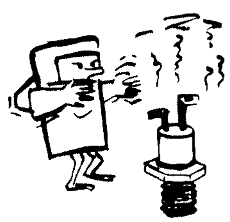
Regardless of how well electrical equipment is designed, personnel can be exposed to **dangerous electrical shock** when protective covers are removed for maintenance or other activities. Therefore, it is incumbent on the user to see that all safety regulations are consistently observed and that each individual assigned to the equipment has a clear understanding of first aid related to electrical hazards.

In addition, the following safety practices must be followed:



1 Do not attempt to adjust unprotected circuit controls or to dress leads with power **on**.

2 Do not touch heavily loaded or overheated components without precaution to avoid burns.



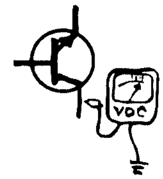


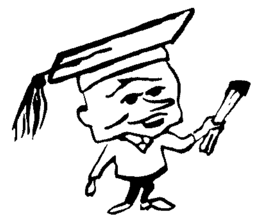
3 Do not assume that all danger of electrical shock is removed when power is off. Charged capacitors can retain dangerous voltages for a long time after power is removed. These capacitors should be discharged through a suitable resistor before any circuit points are touched.

4 Always avoid placing parts of the body in series between ground and circuit points.



5 Remember that some semiconductor cases and solid-state circuits carry high voltages.





6 Don't take chances. Be fully trained. Ampex equipment should be operated and maintained only by fully qualified personnel.

If someone seems unable to free himself while receiving an electrical shock, **turn power off** before attempting to render aid. A muscular spasm or unconsciousness can make a victim unable to free himself from the electrical power.

WARNING

DO NOT
TOUCH VICTIM OR HIS CLOTHING BEFORE
POWER IS REMOVED OR YOU MAY ALSO
BECOME A SHOCK VICTIM

If power cannot be removed immediately, **very carefully** loop a length of dry nonconducting material (such as rope, insulating material, or clothing) around the victim and pull him free of the power. Carefully avoid touching him or his clothing until free of power. Immediately start the appropriate first aid procedures.

GOOD PRACTICES

In maintaining the equipment covered in this manual, please keep in mind the following standard good practices:

1. When connecting any instrument (oscilloscope, waveform monitor, etc.) to a high-frequency output, use the appropriate termination resistor at the input of the instrument, unless the instrument is terminated internally.

2. When inserting or removing printed wiring assemblies (PWAs), cable connectors, or fuses, always turn off power to the affected portion of the equipment. After power is removed, allow sufficient time for the power supplies to bleed down before reinserting PWAs.

3. When troubleshooting, remember that FETs and other metal-oxide-semiconductor (MOS) devices may appear defective because of leakage between traces or component leads on the printed wiring board. Clean the printed wiring board and recheck the MOS device before assuming it is defective.

4. When replacing MOS devices, follow standard practices to avoid damage caused by static charges and soldering.

5. When removing components from PWAs (particularly ICs), use care to avoid damaging PWA traces.

WARNING

This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. As temporarily permitted by regulation it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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SECTION 1
GENERAL INFORMATION

1-1. SCOPE OF MANUAL

This manual contains installation and operating instructions, theory of operation, maintenance instructions, and parts lists and schematics for the VPR-2 series Time Code Reader/Generator Accessory, Kit Part Numbers 1400840 (VPR-2 Serial Nos. 101-399), 1400859 (VPR-2 Serial Nos. 400-1849) and 1400860 (VPR-2 Serial Nos. 1850 and up and all VPR-2B's). The kits include Time Code Reader/Generator printed wiring assembly (PWA) 1400163. The material in this manual is divided into the following six sections:

- Section 1 General Information
- Section 2 Installation
- Section 3 Operation
- Section 4 Theory of Operation
- Section 5 Maintenance
- Section 6 Parts Lists and Schematics

1-2. RELATED PUBLICATIONS

The following publications can be used as reference for the VPR-2 series system in which the Time Code Reader/Generator Accessory is used:

- VPR-2 Character Generator Accessory, Operation and Maintenance Manual, Catalog No. 1809378.
- VPR-2 Installation and Maintenance Manual, Catalog No. 1809379.
- VPR-2 Theory and Maintenance Manual, Catalog No. 1809380.
- VPR-2 Parts Lists and Schematics Manual, Catalog No. 1809384.
- VPR-2B Installation and Operation Manual, Catalog No. 1809519.
- VPR-2B Theory and Maintenance Manual, Catalog No. 1809477.
- VPR-2B Parts Lists and Schematics Manual, Catalog No. 1809472.

1-3. USE OF ACCESSORY

The Time-Code Reader/Generator (TCR/G) PWA accessory provides recording and playback of standard SMPTE/EBU 80-bit time code. The accessory includes two internal time-code generators and two independently resettable tape timers. An externally generated time code may be recorded and displayed, and may also be displayed during playback.

During both playback and record, the accessory provides a time-code output to the Tape Timer PWA and to a character generator accessory, if used. In order to display the time code on the monitor screen, it is necessary to install the Character Generator, Accessory PWA, Part Nos. 1400234 (VPR-2 Serial Nos.101-399) and 1400235 (VPR-2 Serial Nos. 400 and up and all VPR-2B's). When the TCR/G accessory is installed, the time-code output of the accessory is routed to the VPR TIME CODE OUTPUT connector (J19) and to the REMOTE connector. This time-code output is at a constant frame rate when the transport is in slow motion or shuttle. That is, the code is always at a 30-Hz (25-Hz – 625) rate. When the transport is running in slow motion, the 30/25-Hz code only increments proportional to the transport speed, repeating the same code frame number dependent

on the speed. When in shuttle, the 30/25-Hz code will skip some frame numbers.

If an editing system requires standard wideband high speed or slow speed code rates, a jumper can be positioned to provide this signal without affecting the internal time-code reading, generation, or display. However, the internal time-code generator output, and the tape timer signals encoded into the 80-bit SMPTE code are not available at the output of the VPR; only directly off-tape code is available.

1-4. PHYSICAL DESCRIPTION

The Time-Code Reader/Generator Accessory consists of a single, standard VPR-2 Series PWA which plugs into slot 16 of the electronics assembly rack.

1-5. FUNCTIONAL DESCRIPTION

Refer to the simplified block diagram of the TCR/G PWA, Figure 1-1. In the record mode, the time code may be generated in the computer circuit and sent via the output circuit to the Audio PWA, to drive the record head. Time-code geneneration is based on the ref frame, add 1, and 64 X H input signals; the signal information is sent to the computer by means of interrupts. Also, an external time-code generator may be used. Its signal is decoded, processed by the computer, encoded, and routed to the audio board for recording. Either time-code output will be sent to the Tape Timer PWA in a format for display to frames, seconds, minutes and hours. Also, user bit information may be selected for display, in hexadecimal format.

In playback the off-tape time code is applied through decoding circuitry to the computer for processing. It is phased with video, displayed, encoded, and sent off the board for editing purposes.

The mode of operation is selected by means of PWA front edge switches. A microprocessor provides versatility in the presetting and display of time code and user bits for the internal time-code generators. Either tape timer may be selected for display, or independently reset. Time code is displayed over the full forward/reverse shuttle speed range.

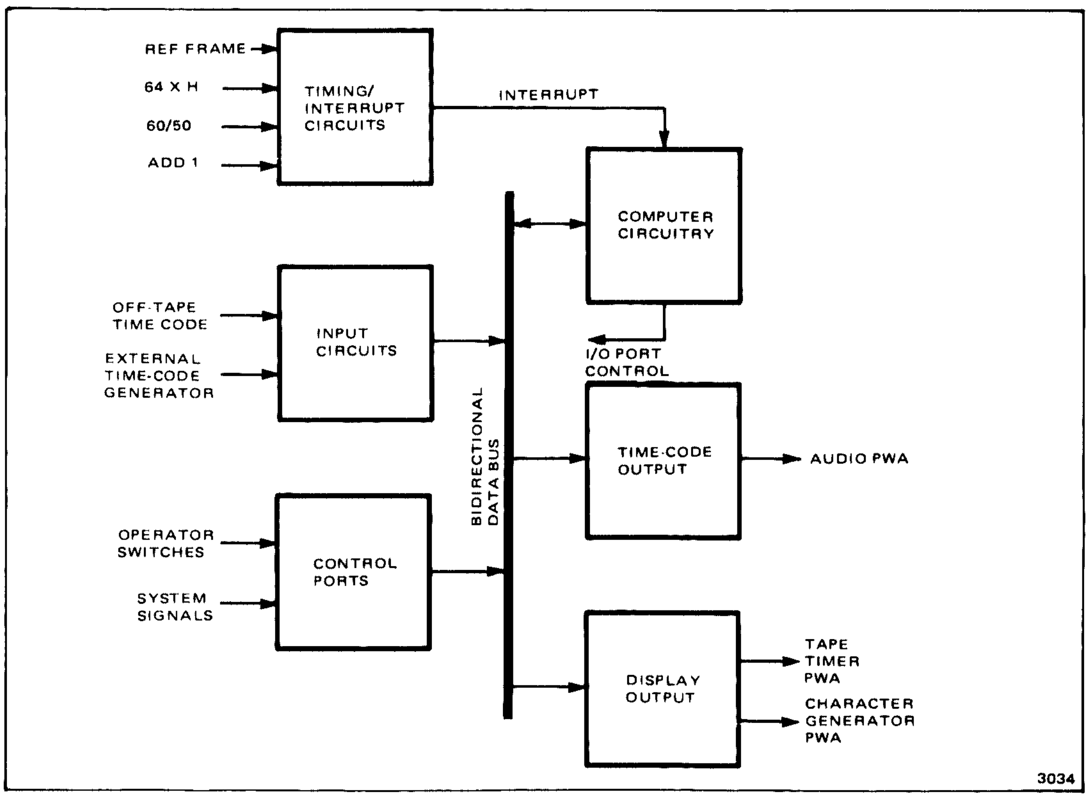


Figure 1-1. TCR/G PWA, Simplified Block Diagram

SECTION 2
INSTALLATION

2-1. INTRODUCTION

This section provides installation instructions for the Time-Code Reader/Generator PWA Accessory. Separate installation instructions are given for two sets of VPR-2 serial numbers.

2-2. UNPACKING

The TCR/G contains MOS devices.

CAUTION

WHEN HANDLING THIS PWA FOLLOW STANDARD PRACTICES TO AVOID DAMAGE TO MOS DEVICES BY STATIC CHARGES AND SOLDERING.

2-3. INSTALLATION

For VPR-2 Serial Nos. 101 through 399, kit No. 1400840 must first be installed. Then plug the TCR/G PWA into slot 16 of the electronics assembly rack. For VPR-2 Serial Nos. 400 through 1850, kit No. 1400859 must first be installed. Then plug the TCR/G PWA into slot 16. For VPR-2 Serial Nos. 1850 and up and all VPR-2B's kit No. 1400860 is supplied and no machine modifications are required. (Note: Installation instructions for installing the kits are given in manual No. 1809457, which is furnished with the kits.)

CAUTION

WHEN REMOVING THE TCR/G PWA FROM ITS SLOT, DO NOT PULL A FRONT EDGE SWITCH KNOB, AS THIS COULD DAMAGE THE SWITCH.

2-4. Jumper Positioning

When the TCR/G kit is installed, two jumper changes on the VPR-2 are required as follows:

1. For 525- or 625-line use, set jumper J6 of the Audio PWA (board No. 2) to the A–B position to provide remote and BNC connector outputs from the TCR/G. (The TCR/G record level output is controlled by the setting of 2R154 on PWA 2, and is factory set for a +2.0 dB reading on the Audio 3 vu meter.) (Note: The TCR/G has a constant frame rate output when the transport is in slow motion or shuttle modes. This output will be at a 30-Hz (25-Hz) rate. If an editing system requires slow or high speed rates (off-tape wide-band code) then jumper J6 should remain in the B–C position.)

2. For a 625-line system with the optional EBU fourth audio channel electronics installed, set jumper J1 of the EBU Audio PWA (board no. 3) to the B–C position to enable acceptance of the TCR/G output.

2-5. Initial Checkout

The TCR/G has had complete factory testing prior to shipment. As a check for possible shipping damage, visually inspect the board for broken or loose component leads and for any damage to printed circuit traces. Then perform the diagnostic self-test per paragraphs 5-2 through 5-7 of this manual.

SECTION 3
OPERATION

3-1. INTRODUCTION

This section contains a table of operator control switches (Table 3-1), a table of the display indicators (located on the tape timer display panel, Table 3-2), and a description of operating procedures, for the TCR/G board.

3-2. TCR/G OPERATION

The operator controls the TCR/G functions by means of PWA front edge switches, and the RESET button on the tape timer display panel. The operating modes of the various switches are described below. Refer to Table 3-1. Also, an example is presented (paragraph 3-19) of operation of the TCR/G during a typical record and playback sequence.

3-3. Preset Switch

In the ADVance position (right), the available display characters will sequence, in the units-frame position, until the switch is returned to center position. If the selected character is not shifted or loaded within about 4 seconds, it will be removed.

In the SHIFT position (left), the selected character will shift, one position per switch actuation, from the units-frame position toward the tens-hour position. When the character reaches the desired position, return switch to center position. If the character is not loaded within about 4 seconds after reaching the desired position, it will be removed.

3-4. Load Switch

The LOAD position (right) is used in conjunction with the PRESET switch. After a preset character is in position, move LOAD switch (within about 4 seconds) to LOAD position. This loads the selected character into an internal microprocessor buffer associated with the displayed function. Repeat this preset/load operation for each desired character change.

The LOAD position is also used to preset the time-code generator to external time code. See paragraphs 3-8 and 3-9. Moving the LOAD switch to the DF/FF position (left) in 525 line use only alternately selects drop frame or full frame operation, as indicated on the tape timer display panel (paragraph 3-19).

3-5. TCR/G Mode Switch

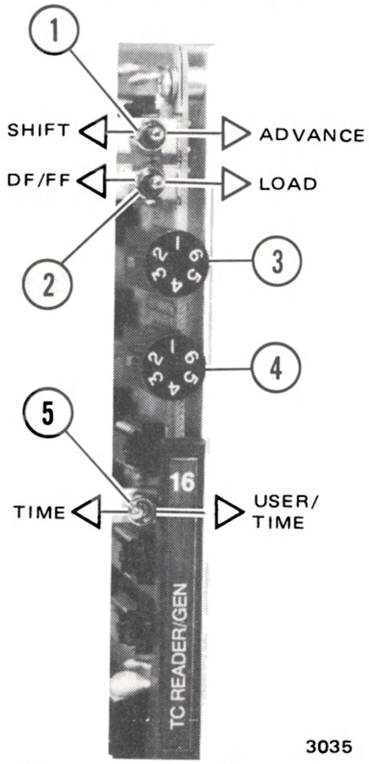
This switch is used to select one of six functional modes described below. The switch position for each mode is given in parentheses, following the name of the mode.

3-6. Timer (1). This position selects tape timer 1 and tape timer 2 outputs, for recording and display. The tape timer 1 values are in the time bit positions of the associated buffers and the tape timer 2 values are in the user bit positions. Either timer may be selected for display, by means of the DISPLAY switch (paragraph 3-18). Also, the timers are independently resettable. The timer selected by the DISPLAY switch is reset to zero when the RESET button, on the tape timer display panel, is pushed.

3-7. TCR (2). This position selects the time-code reader output, for display and for an output for editing purposes. Either the time bits or the user bits may be selected for display, by means of the DISPLAY switch.

3-8. TCG-1 (3). This position selects the TCG-1 output for recording and display. Either the

Table 3-1. TCR/G Operator Control Switches



INDEX NO.	NAME	FUNCTION
1	Preset Toggle Switch (S1)	Used to select preset values.
2	Load Toggle Switch (S2)	Loads preset or external TCG values. Also selects drop frame or full frame.
3	TCR/G Mode Rotary Switch (S3)	Selects one of six TCR/G modes.
4	TCG-1 Mode Rotary Switch (S4)	Selects one of four TCG-1 modes, or test mode.
5	Display Toggle Switch (S5)	Selects time bit position or user bit position for display.

time bits or the user bits may be selected for display. Also, the time bits and user bits may be independently preset, as selected by the DISPLAY switch, and using the PRESET and LOAD switches. (Note that the user bit "alphabet" is limited to letters A through F.)

Moving the LOAD switch to LOAD will preset the TCG-1 to an external time-code generator, time and user bits (unless a character has been selected via the PRESET switch, and the 4-second timeout has not yet occurred).

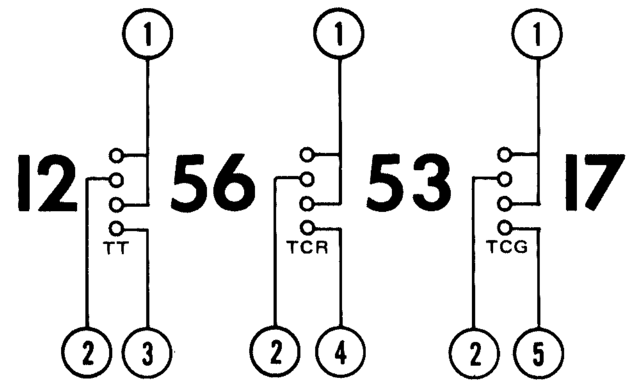
3-9. TCG-1, 2 (4). This position selects the TCG-1 time bits and the TCG-2 time bits (in the TCG-1 user bit positions) for recording and display. The time bits of either may be selected for display by the DISPLAY switch.

The TCG-1 time bits are internally generated only and may be preset to selected values when this generator is selected by the DISPLAY switch. The TCG-2 time bits are continuously sequencing. The TCG-2 value may be preset to an external time-code generator, when selected by the DISPLAY switch. This is done by momentarily moving the LOAD switch to the LOAD position. Or, TCG-2 may be preset to the desired time bit value, using the PRESET and LOAD switches, when selected by the DISPLAY switch. (Note that it continues sequencing during the presetting process.)

3-10. Ext TCG (5). This position selects an external time-code generator, time and user bits for recording and display. The function is not presettable.

3-11. Ext Time (6). This position selects an external time-code generator, time and user bits for recording and display. The user bits may be

Table 3-2. Display Indicators, Tape Timer Display Panel



INDEX NO.	NAME	FUNCTION
1	Colons LED's	Lighted when time bit information displayed; extinguished when user bit information displayed.
2	Drop Frame LED's	Lighted when in drop frame operation; extinguished when in full frame operation.
3	Tape Timer LED	Lighted in tape timer mode. Continuously blinks if there is no control track input.
4	Time Code Reader LED	Lighted in time code reader mode. Continuously blinks if there is no time code input or if it is invalid.
5	Time Code Generator LED	Lighted in time code generator mode. Continuously blinks if the reference video is lost.

preset to selected values when selected by the DISPLAY switch. The time bits are not presettable.

3-12. TCG-1 Mode Switch

This switch is used to select one of four TCG-1 functional modes or the test mode for the TCR/G board. The switch position for each mode is given in parentheses, following the name of the mode.

Switch position 1 is not used, but at present will select the position 2 function (CONTinuous).

3-13. Continuous (2). TCG-1 runs continuously.

3-14. Hold (3). Stops TCG-1 sequencing. When presetting TCG-1, this position facilitates character selection.

3-15. Sequence (4). TCG-1 sequences whenever the audio 3 channel is in record, and stops when it is not in record.

3-16. Jam (5). The time-code reader value is jammed into TCG-1, locking TCG-1 to the time-code reader for assembly operation.

3-17. Test (6). Enables internal PWA diagnostics for the TCR/G. See Section 5, *Maintenance* for diagnostic test procedures. Also, in this position, a manual reset of the TCR/G PWA is produced when the PRESET switch is moved to the ADVance position (right).

3-18. Display Switch

This is a two position switch, TIME (left) and USER/TIME (right). In general, the TIME position selects time bit positions for display, and the USER/TIME position selects the user bit positions (which may hold user or time bits, depending on the mode of operation).

However, with the TCR/G mode switch at position 1 (TIMER mode), the TIME position selects tape timer 1, for reset, recording, and display; the USER/TIME position selects tape timer 2 for these functions. Also, with the TCR/G MODE switch at position 4 (TCG-1, 2), the TIME position selects TCG-1 (time bits only), for preset purposes, recording, and display; the USER/TIME position selects TCG-2 (time bits only) for these functions.

3-19. Operational Example

This example lists operating procedures for recording time code, from a preset starting value, then reading that time code in playback. It also includes the presetting of user bits. Perform this record/play sequence per the following steps:

1. Turn on VPR power.
2. On the TCR/G MODE switch, select position 3 (TCG-1).
3. On the TCG-1 MODE switch, select position 3 (HOLD).
4. Set the DISPLAY switch to the left (TIME).
5. Preset and load the desired starting value for the time code, using the PRESET and LOAD switches as in paragraphs 3-3 and 3-4.
6. Set the DISPLAY switch to the right (USER/TIME).
7. Preset and load the desired user bit information, using the PRESET and LOAD switches.
8. Set the TCG-1 MODE switch to position 4 (SEQUENCE), permitting the time code to sequence only when the audio 3 channel is in record.
9. On PWA 2 of the VPR electronics assembly, set the audio 3 LINE/MIC/TIME CODE switch to TIME CODE.
10. On the VPR control panel, set the AUDIO 3 record switch to the up position, and place the VPR into record mode. (By means of the DISPLAY switch, either the user bits or the time code may be displayed during record.)
11. When recording is completed, rewind to the initial (preset) time code value, and place the machine in stop mode.
12. On the TCR/G MODE switch, select position 2 (TCR).
13. Place the machine in playback.
14. Use the DISPLAY switch to view either the recorded user bits or the recorded time code.

SECTION 4

THEORY OF OPERATION

4-1. INTRODUCTION

This section contains VPR-2 Series and TCR/G interface information, a general description of the TCR/G operation, a circuit block diagram, circuit descriptions, and a software block diagram.

4-2. GENERAL THEORY

The TCR/G is capable of generating time code or generating the time code while locked to an external time-code reference. As shown in the simplified interconnect diagram, Figure 4-1, the restored generated time code is available (via jumper J6 in the A–B position) at the REMOTE connector or the TIME CODE OUT connector.

4-3. NTSC System

In record mode, the restored generated time code from pin 33 of the TCR/G is supplied to S4 in the TC position on PWA 2. This signal is amplified and recorded on the tape. If desired, the TCR/G can be synchronized to an incoming time-code reference signal supplied to pin 43 of the TCR/G. In play mode, switch A23, on PWA 2, is in the tape position, and the off-tape signal is supplied through switch A29 to pin 19 of the TCR/G.

4-4. PAL/SECAM System

For the PAL/SECAM system, EBU Audio PWA 3 is installed. In record mode, the restored generated time code from pin 33 of the TCR/G is routed to PWA 3 and supplied through J1, switch S3 in the TC position, to a record amplifier. The amplified signal is recorded on the tape. If desired, the TCR/G can be synchronized to an incoming time-code reference signal supplied to pin 27 of the TCR/G. In play mode, switch A11 on PWA 3 is in the tape position and the off-tape signal is routed via pin 61 to pin 62 of PWA 2. This signal is then routed through switch A29, and via pin 87 of PWA 2, to pin 19 of the TCR/G.

4-5. TCR/G PWA

The TCR/G PWA reads and generates time code in SMPTE/EBU 80-bit format. This format consists of four time-code bits followed by four user bits, alternately, for bit positions 0 through 63. Bits 64 through 79 are used for the sync word. All data processing and I/O control for the board are provided by computer circuitry which uses an MC6802 microprocessor chip. The microprogram for this device is stored in a separate, 4096 X 8, EPROM. A common, 8-bit, bidirectional data bus provides the interface between the computer and the rest of the TCR/G circuitry. Refer to the TCR/G block diagram, Figure 4-2.

The microprocessor has an internal, 128 X 8, RAM which provides a number of 8-bit operational buffers. Included are input and output buffers, two time-code generator buffers, two tape timer buffers, and two "flywheel" buffers. During both play and record modes the tape timer and flywheel buffers are being incremented, or decremented, at a frame rate by tach pulses, via the add 1 signal. Similarly, the time code generator buffers are incremented, or decremented, by the ref frame signal. Under microprocessor control, these buffers are accessed to provide the display and signal outputs as selected by the operator, using the PWA front edge switches. Selection of a given mode will display and output, the value of the associated buffer. The microprocessor also implements the various operator selections for time and/or user bits. In doing so, it must be able to detect whether data is time code or user bit information; it does this by checking the extent of any successive incrementing, or decrementing.

4-6. Playback Mode. Refer to Figure 4-2 and schematic diagram 1400165. In playback, biphase time code is decoded to non-return-to-zero (NRZ) data and a clock signal, which are then applied to a sync detector. On detection of a valid sync word, the 80 bits are loaded into a FIFO, causing a microprocessor interrupt, inter 4. They are then clocked into the microprocessor, via the bidirectional data bus. The value in the flywheel no. 1 buffer is used for the restored time code output and display. Under microprocessor control, this value is compared to each frame of the incoming time code value. If the values are the same, the flywheel value is used. If the values differ for three frames in a row, the incoming time-code value is jammed into the flywheel no. 1 buffer, updating it. Also, the flywheel value is incremented (or decremented) and phased so the restored time code output will occur in phase with the video framing.

4-7. Record Mode. In record mode, time code is generated within the microprocessor, by manipulation of the time code generator buffers. It is applied in NRZ form through output port A35 to Manchester encoding circuitry. The encoded biphase mark signal is then sent off the board via pin 33, for recording. Simultaneously, it is displayed.

Both time-code generator buffers are incremented at a frame rate by the "early frame" signal, A53-6 on the PWA schematic. This output initiates the inter 1 interrupt signal, causing the microprocessor to increment the values of both buffers. Prior to outputting the values of these buffers, the microprocessor must manipulate the data according to the selected mode of operation. For example, external time code generator values may have to be used together with internally preset user bits (EXT TIME), or, TCG-1 time bits may have to be used together with TCG-2 time bits by placing the latter in the user bit positions (TCG-1, 2), etc.

These microprocessor routines are initiated by operator switch selections, and system status signals, which are applied to control port circuitry (Figure 4-2). The microprocessor regularly looks at each of three 8-bit control port words, by clocking them into its input buffer, one at a time; it proceeds to the appropriate program routine when a change occurs. After all necessary data manipulation, ten 8-bit words of NRZ time code are outputted from the selected buffer, each frame, via output port A35. The output clocking is initiated by the inter 2 interrupt signal, which occurs at a 10 X frame rate.

4-8. Diagnostic Mode. The microprocessor program also includes a diagnostic routine, which is controlled by the operator, in the manner described in Section 5, *Maintenance.* This routine checks about 95% of the TCR/G hardware, and provides diagnostic information via the tape timer display. The routine includes a number of subroutines by which the microprocessor checks each circuit area in turn, and displays the result of each check. In this way, the operator is directed to the specific circuit area of any hardware problem, for simplified troubleshooting.

4-9. Circuit Descriptions

The various functional sections of the TCR/G circuitry are described in the following paragraphs. Refer to schematic diagram 1400165 and to the block diagram of Figure 4-2.

4-10. Biphase Decoder. Figure 4-3 shows eight bits of a Manchester code signal (biphase mark), which includes data and clock components. As shown, a "1" has a midpoint transition, a "0" does not, and there is a transition at every bit period boundary. The decoded NRZ data and clock signals are also shown. The decoder must be able to operate during periods of tape acceleration and deceleration.

The biphase decoder senses ones and zeros by comparing the times between transitions for successive bits. If a time between transitions is greater than 1-1/2 times that for the previous bit, then a zero is detected. When comparing against a zero, if the next time between transitions is less than 3/4 that of the zero, a one is detected. This type of decoding allows for maximum tape acceleration or deceleration. The decoded clock component consists of all the biphase transitions plus transitions denoting 3/4 of the way through zero bits.

The decoder circuit selects one of four biphase signal sources: Biphase TC from the audio board, an external audio 3 time code (NTSC), an external EBU audio 3 preamp time code (EBU), or a

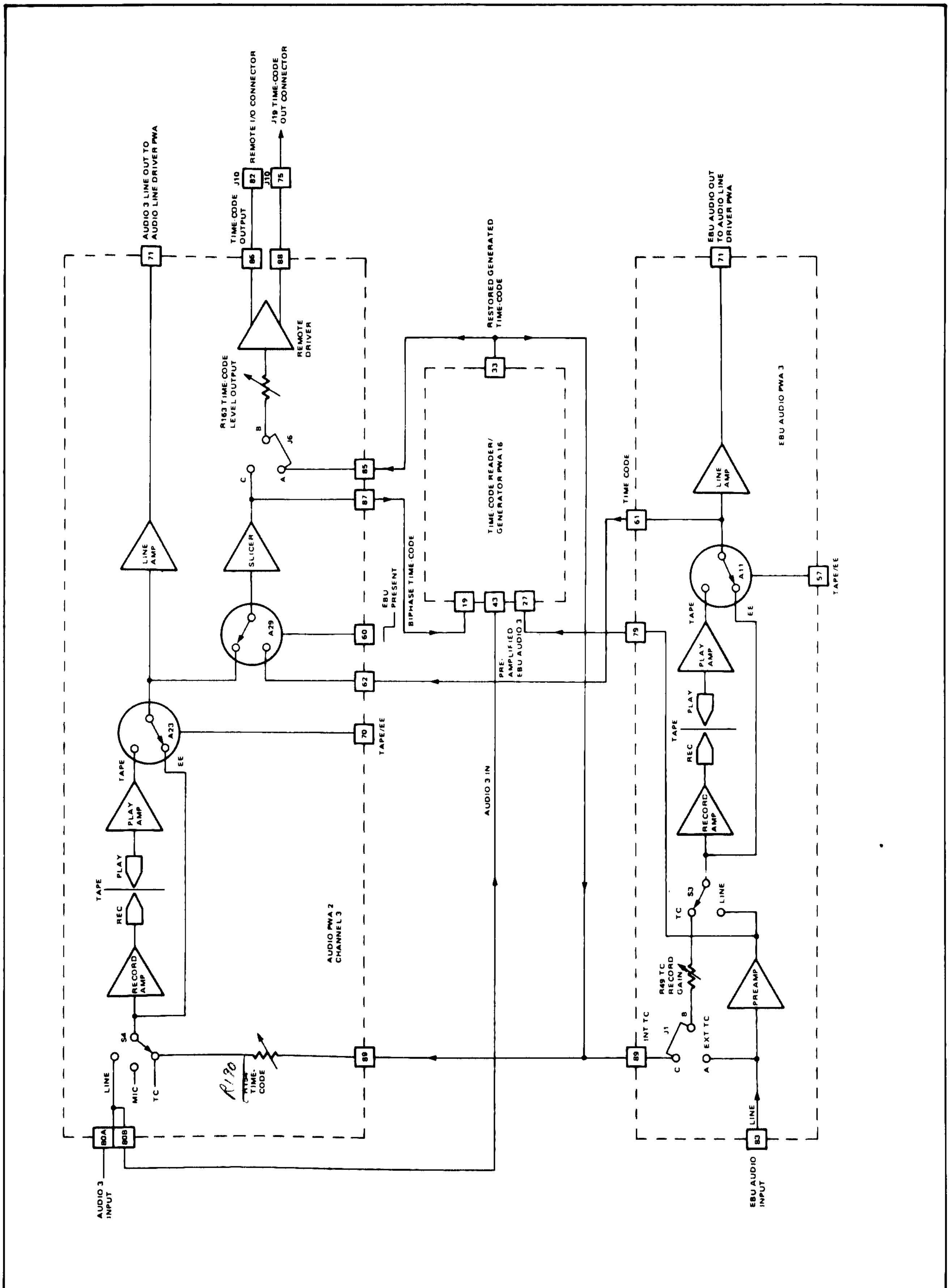


Figure 4-1. VPR-2 Series/Time Code Reader Generator, Simplified Interconnect Diagram

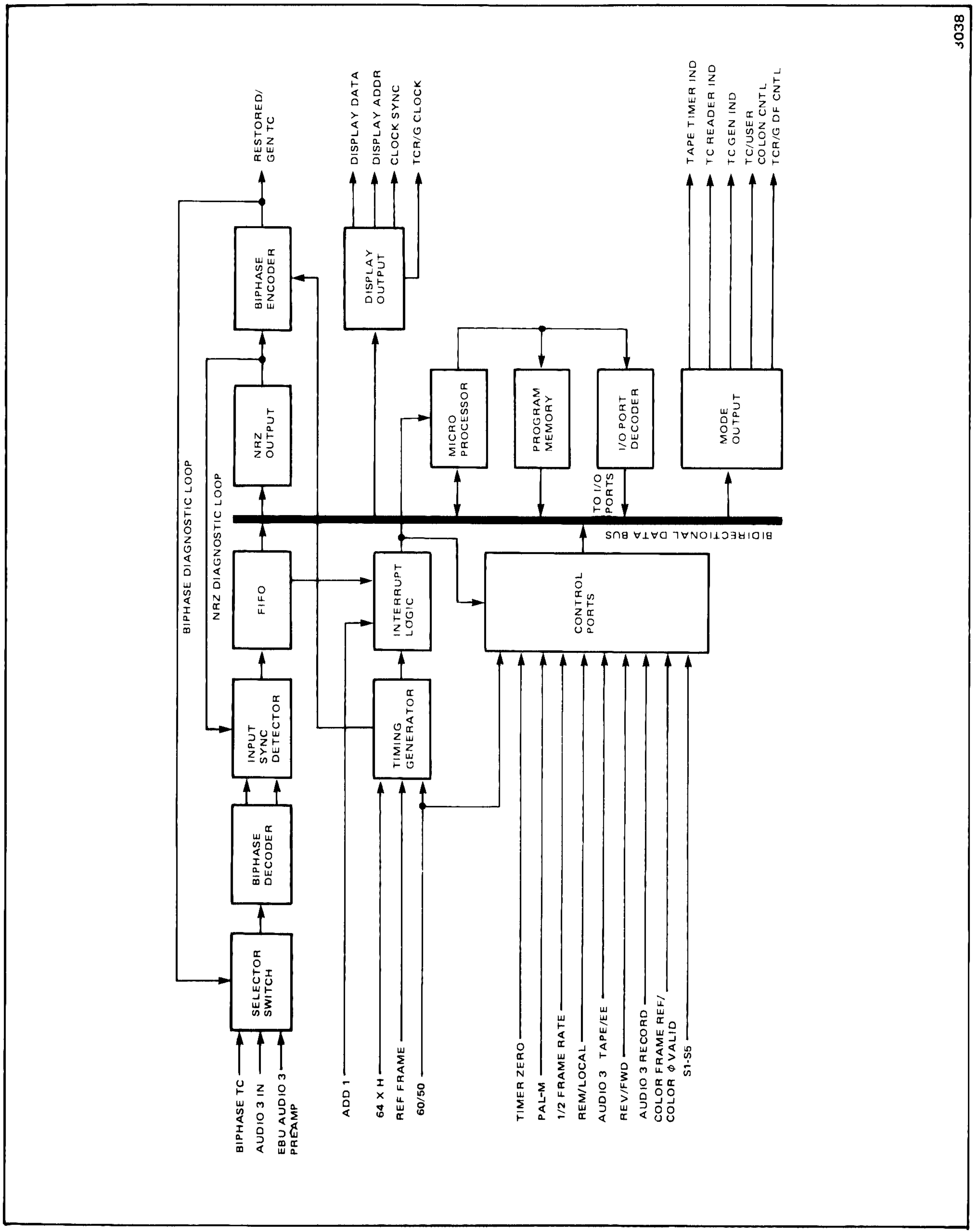


Figure 4-2. TCR/G Block Diagram

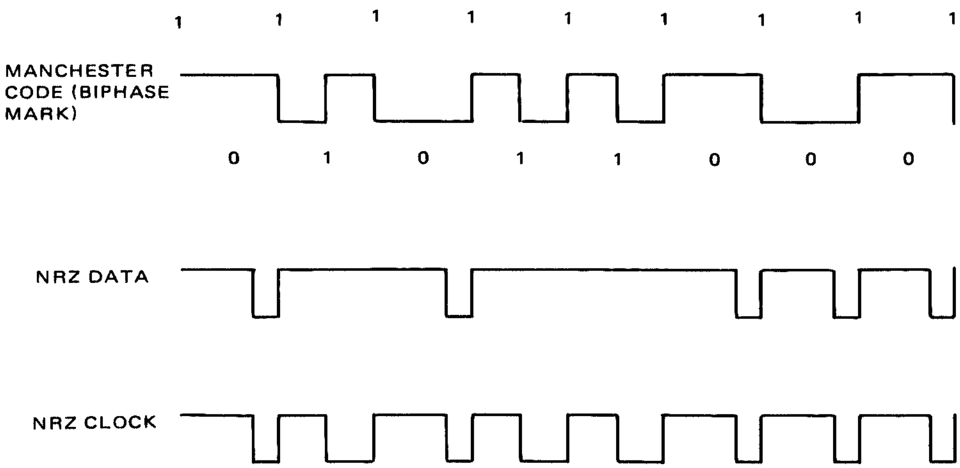


Figure 4-3. Manchester Code

feedback time-code signal used for diagnostic purposes. If an external time code is selected, the presence of an EBU head causes selection of the EBU audio 3 preamp signal.

The selected signal is applied to control circuitry consisting of a decoder control PROM (A15) and an octal latch (A8). The decoder circuitry is clocked by a 4-MHz oscillator (A32) which is not synchronous with the incoming time-code signal. PROM A15 controls two sets of counters to compare the times between transitions, for successive biphase bits. The output of the first set of counters (A4-7) is applied to a set of PROM's (A12-14) which transforms the count to 3/2 its value, if a one, or to 3/4 its value, if a zero. The new value is then loaded into a set of down counters (A18-21) and compared to the time between transitions for the next successive bit. An output from the down counter (A18-13) denotes its value has been counted down to zero before completion of counting of the next successive bit, thus indicating a zero for the next bit. If a transition is reached in the next bit, before the down counter output occurs, a one is detected. Therefore, the PROM uses the down counter output and incoming signal transitions for detecting ones and zeroes.

Also, the clock component of the biphase signal is generated by the decoder control PROM, based on the incoming signal transitions and the down counter output. The resulting NRZ data and the clocking signal for it are applied to a selector (A11). The two signals are passed to the input sync detector circuit, except during a diagnostic test which selects a feedback NRZ signal, and its clocking signal.

4-11. Input Sync Detector and Buffer. Each frame of incoming SMPTE/EBU time code consists of a 16-bit sync word and eight data bytes. The 16-bit sync word includes 12 successive ones and two bits at each end of the word for identifying the direction of tape movement.

The decoded data (selected by A11) is applied to an address line of the sync detector PROM (A3). The outputs of this PROM are applied to the other eight of its nine address lines, via an octal latch which is clocked by the NRZ data clock. The PROM operates as a counter, to detect the 12 successive ones which identify a sync word.

The decoded data is also clocked into a shift register (A9) for grouping into 8-bit bytes. The data is right-shifted in or left-shifted in, as controlled by the FIFO control PROM (A2), depending on the tape direction bits in the sync word. This properly orients the byte for FIFO storage, and eventual data bus transmission.

When a sync word is detected, the FIFO control PROM causes clocking of the sync word and 8-bit data bytes into the FIFO (A17,25). When the ten 8-bit bytes are in FIFO, an interrupt is sent (A1-7) to the microprocessor (A47), indicating the FIFO data is ready. As this is not a high priority interrupt, the FIFO may continue to fill and overflow. An overflow generates a signal (A17-2) which results in clearing of the sync detector latch (A10). This causes proper rephasing of the circuit, to incoming data.

The microprocessor responds to a FIFO interrupt by successively clocking the first ten 8-bit FIFO bytes onto the data bus, and clocking the eight data bytes into the microprocessor RAM (via the microprocessor's accumulator buffer, Figure 4-4).

4-12. Timing Generator. As the time-code output must be phased to video, the timing generator receives a 64 X H clock from the Reference PWA, and a reference frame signal from the Control Track PWA. These signals are used for providing phased timing signals to the rest of the board.

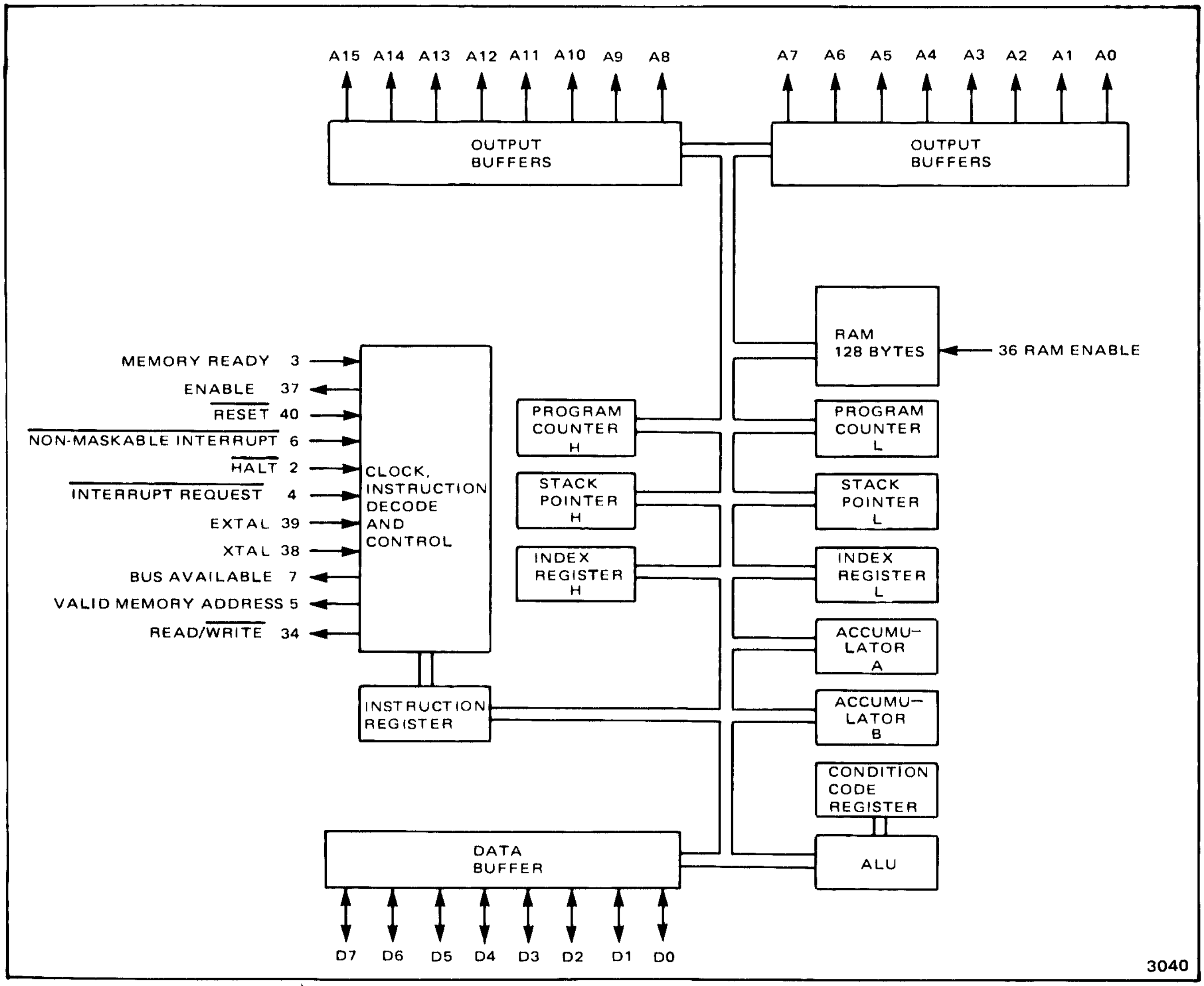


Figure 4-4. Microprocessor Block Diagram

The timing generator consists of a counter chain (A44,46,54,55) clocked by the 64 X H signal (pin 39) and logic for phasing the counter to the ref frame input signal (pin 59). The circuit outputs include two interrupts, inter 1 ("early frame") and inter 2 (10 X frame). Also, phased clock signals are provided for the output buffer (A35), the biphase encoder (A26,34), and two control port buffers (A16,24).

4-13. Interrupt Logic. This circuit consists of latches for each of four interrupt signals and a priority interrupt encoder PROM. An interrupt clocks the associated latch, applying a zero to the PROM. The PROM outputs an interrupt request (IRQ) to the microprocessor and provides two bits to a buffer (A36) to identify which of the four interrupts occurred. The interrupt is cleared by the microprocessor via the interrupt acknowledge latch (A28).

4-14. Input Ports. The input ports consist of the control ports (A16,24,36) and the FIFO time code buffer (A17,25). The outputs of these ports are applied to the data bus under microprocessor control and clocked into the microprocessor RAM.

Control port latch A16 holds four coded bits defining the states of switch S1 (PRESET) and S2 (LOAD). The other four bits in the latch are control bits representing timer zero (pin 40), PAL-M (pin 69), 1/2 frame rate (pin 61), and REM/local (pin 37). Jumper J2 normally grounds the REM/local bit, indicating local control of the VPR, rather than remote control. The remote control position of J2 is described in jumper Table 5-1.

Control port latch A24 holds three bits defining the selection made via the TCR/G mode switch S3 and three bits associated with the TCG1 mode switch S4. This latch also holds two bits for the USER/TIME switch S5. Control port latch A36 holds three bits of interrupt information and five bits from board input signals: 60/50, AUD 3 TAPE/EE, REV/FWD, COLOR FRAME REF/COLOR ϕ VALID, and AUD 3 REC.

The 16 byte FIFO buffer (A17, 25) used for time code data generally holds 10 bytes at a time. The extra storage capacity allows for delays in interrupt acknowledgments and for varying speeds of NRZ data input, with varying tape speeds.

4-15. Output Circuits. The display output circuit consists of output ports A37,45 and display addressing logic A26,27,30,38,42,50. A37,45 are 4-by-4 register files. Four data bus bits are written into the 4-by-4 register files using the write port under microprocessor control. Four display output bits are read from each register file using the read ports. Writing and reading can occur simultaneously. The sequential read addressing is provided by counting circuitry clocked from the microprocessor. The counting circuitry also sends the display address to the character generator, a clock signal to the character generator and the tape timer, and sends a clock sync signal to the tape timer. The output display data is sent on four lines to the character generator and the tape timer.

The time-code output circuit consists of a parallel-in, serial-out, register (A35) that feeds a Manchester biphase mark encoder consisting of two exclusive-OR gates and a flip-flop. The encoded output is sent to the audio board via pin 33, as the restored/ gen TC signal. For diagnostic purposes, the NRZ data (A35-9) may be fed back into the input sync detector and the encoded Manchester output (A34-6) may be fed back into the biphase decoder.

The output "mode port" A28, holds four mode display bits and four interrupt acknowledge bits. Two of the mode display bits are applied to a mode display control PROM (A29). The PROM receives these and other control bits and provides output signals to LED mode indicators for the tape timer, TC reader, and TC generator (see Section 3, *Operation*). The other two mode display bits from A28 provide a TCR/G drop frame control signal and a TC/USER control signal. The four interrupt acknowledge bits are used to clear the four IRQ interrupt latches.

4-16. Computer Circuitry. The computer circuitry consists of a microprocessor (A47), a program memory EPROM (A40), and an I/O control decoder (A39). The computer provides data processing and I/O control for the TCR/G board. The program memory EPROM is addressed by microprocessor address and enable lines, and

provides instruction words to the microprocessor in 8-bit bytes via a common bidirectional 8-bit data bus. The I/O control decoder receives address bits and enable signals from the microprocessor to enable the various I/O ports tied to the common data bus.

4-17. Microprocessor. The MC6802 (A47) is an 8-bit microprocessor having an internal 128 byte RAM. The principal operational buffers for the TCR/G program are located in this RAM to allow for direct addressing. The 6802 chip includes all the circuits required for fetching, interpreting and executing the instructions stored in EPROM A40, except for the I/O decoding function provided by A39.

A block diagram of the microprocessor is presented in Figure 4-4. The device has three 16-bit registers (program counter, stack pointer, and index register) and three 8-bit registers (condition code register, and accumulators A and B) available for use by the programmer. Output buffers provide for 16 address bits, three of which are not used in this application. Appropriate control signals apply these address bits either internally to the RAM, or externally to the EPROM program or the I/O decoder. The 8-bit data buffer is bidirectional, transferring data to and from the memory and peripheral devices. The data bus is placed in output mode when the RAM is accessed, preventing external data from entering the microprocessor. Refer to the MC6802 data sheets for a detailed description of the microprocessor architecture, timing, and signals.

4-18. EPROM and I/O Decoder. The microprocessor program is stored in a 4096 X 8 eraseable programmable read only memory (EPROM) (A40) which is addressed by lines A0 through A12. Lines A4 through A7 also address the I/O decoder (A39).

The microprocessor uses "memory mapping" to access the appropriate hardware device (internal RAM, program EPROM, or I/O decoder A39) for implementing a program instruction or for fetching the next instruction. It looks at each of these devices as a block of (hex address) memory locations. The RAM has addresses 00 through 7F, the I/O decoder is 80 through F0 (with some unused locations), and the EPROM microprogram has addresses 1000 through 1FFF. Additional enabling signals (E, VMA) and gating (A31) provide for enabling of only one of these devices at a time. For example, I/O decoding will occur only if line A7 is high (above address 007F), and the EPROM will be enabled only if line A12 is high (hex address 1000 or higher). Addressing the EPROM places one byte of an instruction word onto the common data bus, for input by the microprocessor. One-, two-, and three-byte instruction words are used. Addressing the I/O decoder causes enabling of an I/O port, except for output A39-9, which clears the FIFO port.

4-19. MICROPROCESSOR PROGRAM

Refer to Figure 4-5, microprocessor program block diagram. The microprogram basically consists of an initialize routine, an idle routine, an interrupt service routine, and four interrupt routines. It also includes a diagnostic program for self-checking of the TCR/G hardware, and time code incrementing and decrementing subroutines (not shown in Figure 4-5).

The initialize routine is initiated by a reset pulse (A47-40), which has priority over all interrupts. This routine includes basic housekeeping functions such as clearing the internal RAM to all zeros, setting the stack pointer, and clearing the interrupts. The program then goes into idle mode, which includes such routine functions as setting the mode indicators, loading sync bytes into the output buffer, and controlling preset operations, while waiting for an interrupt to occur.

The highest priority interrupt is NMI (nonmaskable interrupt). This is a hardware interrupt which enables the PWA diagnostic program. Next in priority is a software interrupt, SWI. The lowest priority interrupt is a hardware interrupt request, IRQ (A47-4).

IRQ can be produced by any of four hardware interrupt signals. Inter 1, the highest priority of these four, is initiated by the "early frame" signal, and is needed for correct phasing of time code to video. Inter 2, next in priority, is initiated by a

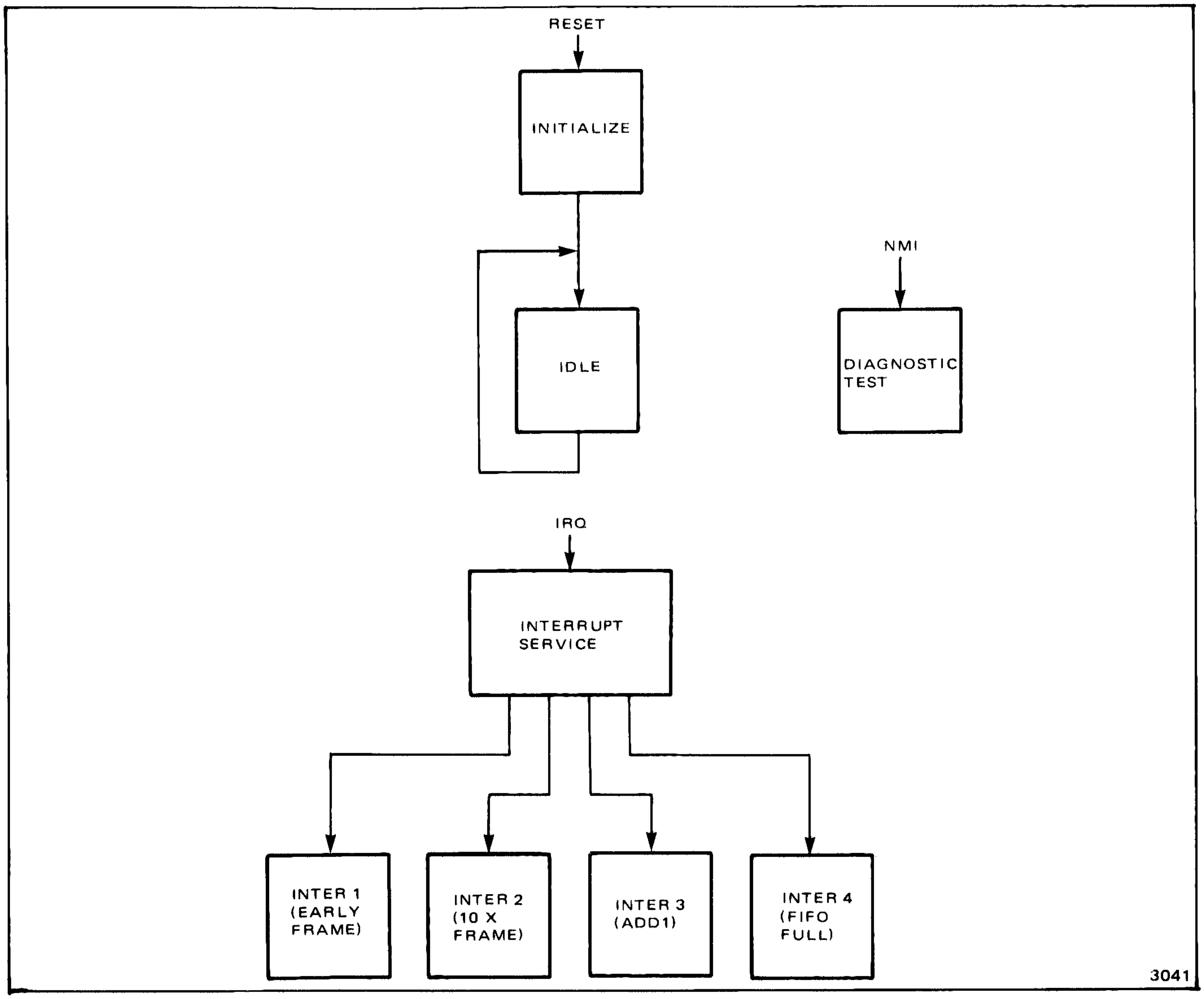


Figure 4-5. Microprocessor Program Block Diagram

10 X frame signal, and is also used for correct phasing. The inter 3 signal, initiated by the add 1 signal, causes updating of the tape timers and flywheels. Inter 4, with the lowest priority, notifies the microprocessor that the input FIFO port is filled, with NRZ data.

As an example of an interrupt program routine, the inter 3 program accomplishes a number of functions needed to sequence the tape timers. It operates on tape timer 1, tape timer 2, flywheel 1, and flywheel 2, in that order. Starting with tape timer 1, it checks for full frame or drop frame operation and loads an index register for addressing. It tests tape direction and jumps to an increment routine for forward direction or a decrement routine for reverse direction. The increment or decrement routine checks for 525 or 625 line use, increments or decrements the units-frame value by one, and checks the other character values as needed to provide the proper carry operations. When this subroutine is complete, the program proceeds to tape timer 2, then to flywheels 1 and

2. Finally, the program returns to the idle routine to wait for another interrupt.

Similarly, the inter 1 routine manipulates the RAM operational buffers as required by the mode selection switches, prior to display and output. The inter 2 routine causes storing of the appropriate buffer values into the output port (A35), at a 10 X frame rate. The inter 4 routine includes inputting of FIFO data into a time code buffer, comparing it with the flywheel value, and correcting the flywheel if necessary.

An interrupt program routine is stopped when a higher order interrupt occurs. The next instruction address of the stopped routine is stored in the "stack" register, in RAM. After completion of the higher order routine, the stopped routine resumes, by retrieving its next instruction from the stack and proceeding from that point. Several in-process interrupt routines can be stopped, at a given time, due to successively higher priority interrupts occurring. They will be resumed in reverse order of their stopping, as the stack is operated in a first-in, last-out manner. The stack register consists of RAM locations 5B through 7F.

SECTION 5
MAINTENANCE

5-1. INTRODUCTION

This section contains maintenance information for the Time Code Reader/Generator PWA. The section includes jumper and test point tables and test procedures (Tables 5-1, 5-2) for using the TCR/G diagnostic program. Refer to Figure 5-1 for jumper and test point locations.

5-2. TCR/G DIAGNOSTIC SELF-TEST

The microprocessor program includes a diagnostic routine for checking the TCR/G hardware. This diagnostic is operator controlled, via PWA front edge switches, and displays the test results on the tape timer display panel. Step-by-step procedures for operating this diagnostic test are listed below. The test should be performed only in the sequence as given. Before starting the diagnostic, turn power off, remove the TCR/G board and position it on an extender, then insert the extender into slot 16.

5-3. Display Check

This test includes a check of all RAM locations, of some microprocessor operations, and of the TCR/G display output circuitry. Also, steps 7 through 11 test the operation of the mode port circuits, A28 and A29. Perform the test per the following steps:

1. Turn VPR power on and place the machine in the stop mode.
2. Set the TCG/R switch (S3) to position 1. Set the DISPLAY switch (S5) to the TIME position (left).
3. Set the TCG-1 mode switch (S4) to position 6, to enable the diagnostic program.
4. Momentarily press the LOAD switch (S2) at the LOAD position (right). The program then tests all RAM locations, some of the microprocessor operations, and the zero bits of the display output circuit. The tape timer display should show all zeros, and the tape timer LED should be on.
5. Move the PRESET switch (S1) to the SHIFT position (left), then return it to center-position. The display should show all ones, with the tape timer LED on.
6. Repeatedly move the PRESET switch to the SHIFT position, sequencing the display to all 2's, 3's, etc., until all F's are displayed. The tape timer LED should be on, with each set of numbers.
7. Move the PRESET switch to SHIFT position (left), momentarily. The display should show all F's, with the TCR LED blinking.
8. Move the PRESET switch to SHIFT again. The display should show all F's, with the TCG LED on.
9. Repeat step 8. The display should show all F's, with the TCG LED on.
10. Repeat step 8. The display should show all F's, with the TCG LED on, and all three sets of colons should be lighted.
11. Momentarily move the LOAD switch to the DF/FF position (left). The display should show all F's, with the TCG LED on, the colons on, and all three drop frame LED's (at centers of colons) on.

Table 5-1. Jumpers

JUMPER	POSITION	FUNCTION
J1		Color phasing
	A–B	Normal position.
	B–C	For possible future use; color phasing per color correction signal.
J2		Local/Remote
	A–B	Normal (local control).
	B–C	Remote control use:
		In remote, and EE – TCG mode only.
		In remote, and TAPE – TCR mode only.

Table 5-2. Test Points

TEST POINT	DESCRIPTION
TP1	Scope trigger for mode port check (A28).
TP2	Scope trigger for control port check (A24).
TP3	Scope trigger for control port check (A16).
TP4	Scope trigger for time code input port check (A17, 25).
TP5	Scope trigger for control port check (A36).
TP6	Scope trigger for time code output port check (A35).
TP7	Scope trigger for display port check (A37).
TP8	Scope trigger for checking input port clearing (A17, 25).
TP9	Ground reference for other test points.

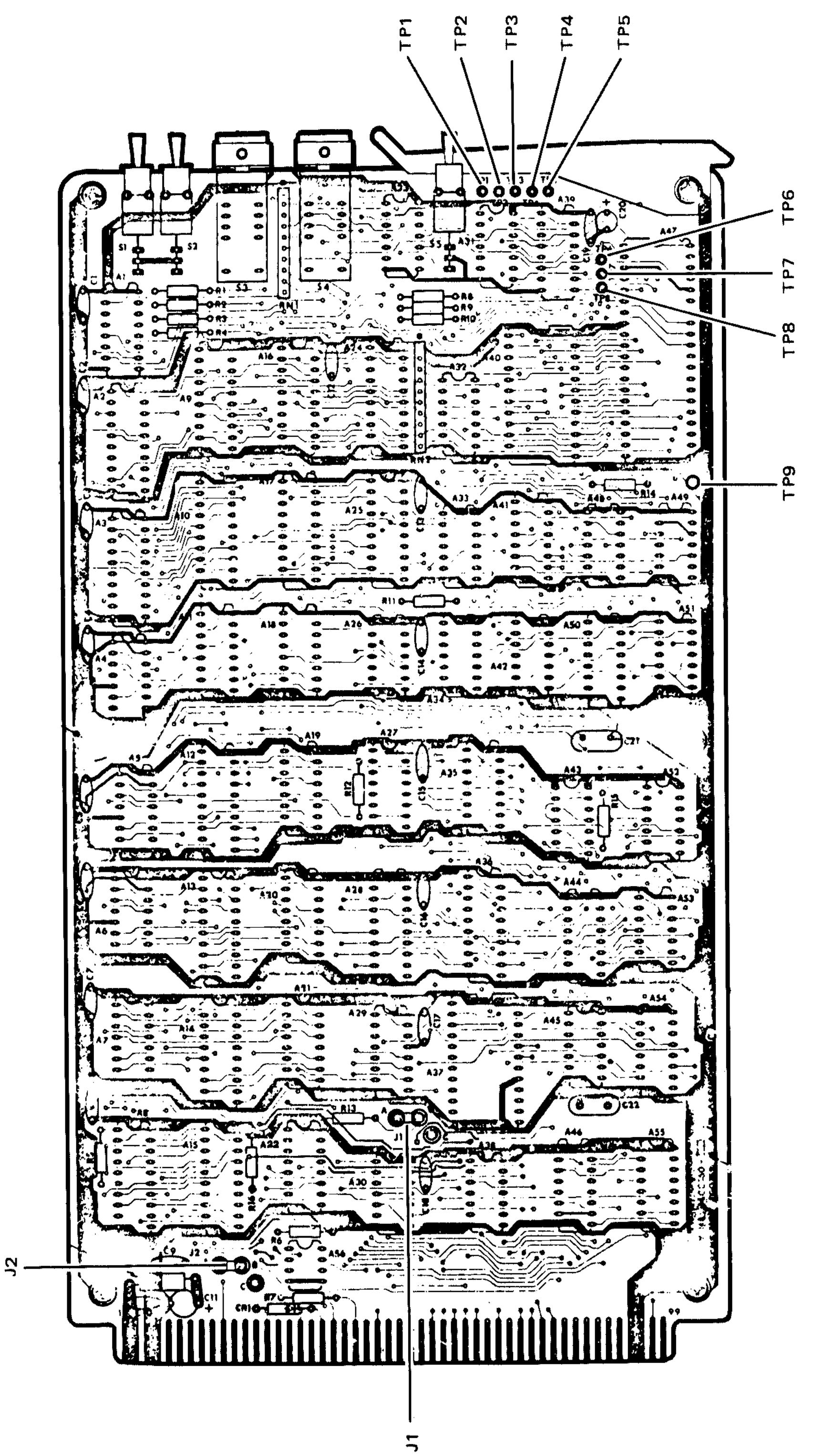


Figure 5-1. TCR/G PWA 16, Assembly No. 1400163

5-4. Control Port Checks

These checks verify control port circuitry, by sending mode selections, via A24, to the microprocessor, then checking the resulting microprocessor outputs. With the VPR-2 still in stop mode, perform the following steps:

1. Momentarily move the PRESET switch to the SHIFT position (left). The display should show all 1's. Ignore all other LED's.

2. Rotate the TCR/G mode switch (S3) through all its positions. At each position, the display should show the number of that switch position. Then set the switch to position 1.

3. Move DISPLAY switch to USER/TIME position (right). The display should show all 6's.

4. Rotate the TCG-1 mode switch (S4) through all its positions. At each position the display should show the number of that switch position. Then set the switch to position 6.

5-5. Functional Test

This test checks the interrupt logic and associated circuitry, including some of the A36 lines. Incrementing and decrementing of the tape timer and flywheel buffers, due to the add 1 pulse, is verified. Load a tape, put the machine in play mode, and perform the following steps:

1. Place the VPR-2 into slow motion (approximately 1/10 normal speed), then momentarily set PRESET switch to SHIFT position (left). The least significant display position should start sequencing from zero through F. Adjust the slow motion knob for a convenient speed. The same sequencing should then occur, in turn, for each of the remaining display positions. After the tens-hour position has sequenced, the sequencing will start again in the unit-frame position.

2. Set the slow motion knob to the reverse jog position. Verify that each display position sequences in the reverse order of step <u>1</u>, above.

5-6. NRZ/Biphase Test

This routine tests the NRZ loop first, then the biphase loop (Figure 4-1). The microprocessor generates a time code number, routes it through output buffer A35 and through the NRZ loop, then reads it from the FIFO (A17, 25). It repeats this for a simulated reverse tape motion. Next, it encodes the time code number and sends it through the biphase loop, then reads the resulting NRZ data from the FIFO. It repeats this for a simulated reverse tape motion. The test is performed as follows:

1. Place the VPR-2 in stop mode. Using a jumper wire with alligator clips, ground pin 50 of the TCR/G board to a convenient ground point such as TP9.

2. Momentarily move the PRESET switch to SHIFT (left). For a successful test, the display will show: 00 00 GOOD.

3. If the test is not successful the display will show: 00 00 XBAD.

4. X will be 1, 2, 3, or 4, where 1 and 2 apply to the NRZ test and 3 and 4 apply to the biphase test, as follows-

   a. 1BAD: FIFO not filled, or FIFO filled but inter 4 interrupt did not occur.

   b. 2BAD: same as 1BAD, but for reverse tape direction.

   c. 3BAD: indicates problem in biphase decoder or biphase encoder.

   d. 4BAD: same as 3BAD, but for reverse tape direction.

5-7. Return to Main Program

When the diagnostic test is completed, return to the main microprogram by one of two methods:

1. Turn power off, remove the extender, remove the jumper that connects pin 50 to ground, and replace the TCR/G into slot 16. Set the

TCG-1 mode switch to the desired operating position, and turn power on.

2. If the board is to be left on the extender, return to the main microprogram by manually resetting the TCR/G board. Do this by moving the PRESET switch to ADVance (right). Remove the jumper that connects pin 50 to ground, and set the TCG-1 mode switch to the desired operating position.

5-8. TIME CODE LEVEL ADJUSTMENTS

If required, perform the following time code level adjustments on the Audio PWA 2, and EBU Audio PWA 3.

1. Remove power and extract Audio PWA 2. Place PWA on an extender board and insert into slot 2.
2. Set switch S4 on PWA 2 to TC (time code) position.
3. Set VPR-2 front panel TAPE/EE switch to EE position.
4. Apply power and adjust TC level input potentiometer ~~R154~~ for +2 reading on the front panel vu meter. R190
5. Connect scope to pin 86 of the PWA and adjust R163 for 4.0 Vp-p.
6. Remove power, remove extender board, and reinstall PWA 2 into slot 2.
7. With power off, extract EBU Audio PWA 3. Place PWA on an extender board and insert into slot 3.
8. Check that jumper J1 is in the B–C position (INT TC).
9. Set switch S3 to TC (time code) position.
10. Check that TAPE/EE switch is in the EE position.
11. Apply power and adjust TC record gain potentiometer R49 for +2 reading on the front panel vu meter.
12. Remove power, remove extender board, and reinstall PWA 3 into slot 3.

SECTION 6

PARTS LISTS AND SCHEMATICS

This section of the manual provides parts lists, assembly drawings and schematic diagrams for the VPR-2 series Time Code Reader/Generator Kit Accessory, Part Nos. 1400849 (VPR-2 Serial Nos. 101-399), 1400859 (VPR-2 Serial Nos. 400-1849), and 1400860 (VPR-2 Serial Nos. 1850 and up and all VPR-2B's).

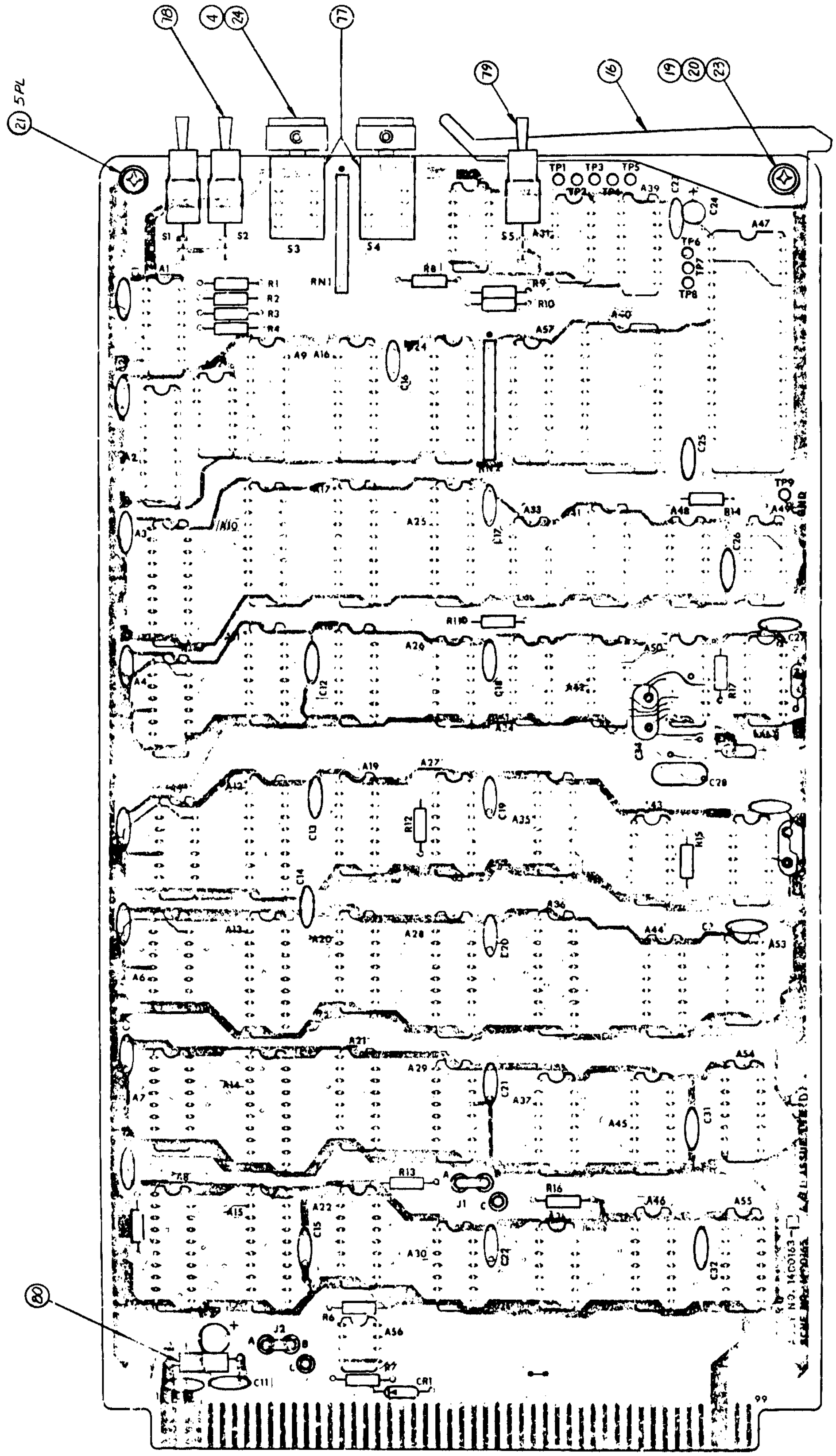
TABLE OF CONTENTS

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02	-03
1	1400160-10	PWA, TC READER/GENERATOR		1	-	-
2	1400163-01	PWA, TC READER/GENERATOR			1	-
3	1400190-07	PWA, TAPE TIMER		1	1	1
4	1400163-04	PWA, TC READER/GENERATOR				1
5	1400420-05	PWA, TIME READOUT		1	1	1
6						
7	1400454-02	FILTER, READOUT		1	1	1
8						
9	1400599-01	KIT POWER SUPPLY UP GRADE		1	1	1
10						
11	1400842-01	MODIFICATION HARNESS		1	1	1
12	1809473	POCKET INSTRUCTIONS		1	1	1
13	1809449	TC READER/GENERATOR ACCESSORY MANUAL OPERATION AND MAINTANENCE		1	1	1
14	1809457	INSTALLATION INSTRUCTIONS		1	1	1
15	302-335	STRAP CABLE, 4"		10	10	10
16	615-094	WIRE INSULATED, 26 AWG		5'	5'	5'
17						
18	1400513-07	LABEL, DOOR		1	1	1

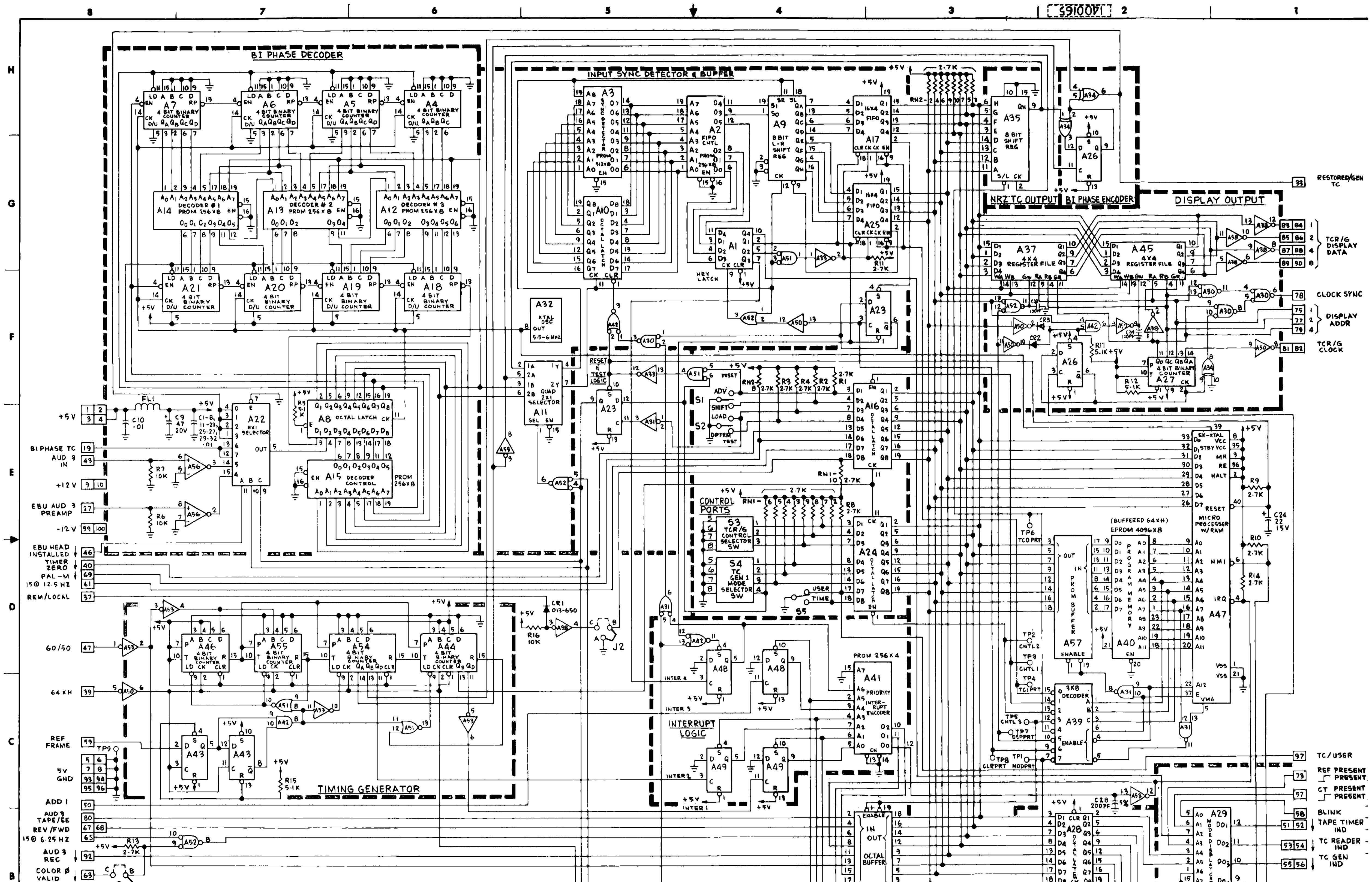
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	-01	-02	-03	-04
1				-01	-02	-03	
2	1400165	SCHEMATIC		[illegible]	A	C	D
3							
4	1400261-02	KNOB, MACHINED	REF: S4	2	2	2	2
5	1400300	PROM, TCRG PRGM ▷1	A40	-04	-05	-06	-06
6	1400301	PROM, BI PHASE DECODER CNTL	A15	-01	-01	-01	-01
7	1400302	PROM, BI PHASE DECODER 1	A14	-01	-01	-01	-01
8	1400303	PROM, BI PHASE DECODER 2	A13	-01	-01	-01	-01
9	1400304	PROM, BI PHASE DECODER 3	A12	-01	-01	-01	-01
10	1400305	PROM, SYNC DETECTOR	A3	-01	-01	-01	-01
11	1400306	PROM, FIFO CONTROL	A2	-01	-01	-01	-01
12	1400307	PROM, INTERRUPT CONTROL	A41	-01	-01	-01	-01
13	1400308	PROM, MODE DISPLAY CONTROL ▷1	A29	-01	-01	-01	-01
14							
15	1400003-01	SHIELD		1	1	1	1
16	1400004-01	EJECTOR, HANDLE		1	1	1	1
17	1400005-AS	LABEL		1	1	1	1
18	506-011	WASHER, BOWED		1	1	1	1
19	283-105	SPACER, PLAIN .140 ID, .250 OD, .125 LG.		1	1	1	1
20	471-063	SCREW,MACH,PAN HD, #4-40 X .438 LG.		1	1	1	1
21	474-500	SCREW,MACH,PAN HD, ASSEM WASH, #4-40 X .312 LG		5	5	5	5
22							
23	502-002	WASHER, SPLIT LOCK #4		1	1	1	1
24	477-672	SCREW,SET #4-40 X .188 LG		2	2	2	2
25	034-286	CAPACITOR,MICA 200PF 5%	C23	1	1	1	1
26	037-954	CAPACITOR,TANT DIP 22UF 15V	C24	1	1	1	1
27	037-892	CAPACITOR,TANT DIP 47UF 20V	C9	1	1	1	1
28	064-116	CAPACITOR,CER DISC .01UF,	C1-8,10-23,25-27,29-32	29	29	29	29
29	034-177	CAPACITOR, MICA, 100PF, 500V. 5%	C33,34			2	2
30	051-770	CHOKE, FERRITE	FL1	1	1		1
31							
32	013-650	DIODE	CR1,2,3	3	3	3	3
33	039-231	RESISTOR,NETWORK 2.7K	RN1,2	2	2	2	2
34	066-666	RESISTOR,C.F. 2.7K 1/4W 5%	R1-4,8-11,13,14	10	10	10	10
35	066-668	RESISTOR,C.F., 4.7K OHMS, 1/4W, 5%	R17	1	1	1	1
36	066-830	RESISTOR,C.F., 10K OHMS, 1/4W, 5%	R6,7,16	3	3	3	3
37	066-842	RESISTOR, C.F., 5.1K OHMS, 1/4W, 5%	R5,12,15	3	3	3	3

AMPEX	Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO 92739	LIST OF MATERIALS	LM-1400163 SHEET 2	REV E

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	-01	-02	-03	-04
38							
39	587-510	INTEGRATED CIRCUIT, 74LS00	A31	1	1	1	1
40	587-750	74LS02	A51	1	1	1	1
41	587-533	74LS04	A38,50,53	3	3	3	3
42	587-902	74LS05	A33	1	1	1	1
43	587-534	74LS08	A42	1	1	1	1
44	587-523	74LS32	A30,52	2	2	2	2
45	587-387	74LS74	A23,26,43,48,49	5	5	5	5
46	587-746	74LS86	A34	1	1	1	1
47	587-279	74LS138	A39	1	1	1	1
48	587-950	74LS151	A22	1	1	1	1
49	587-760	74LS157	A11	1	1	1	1
50							
51							
52	587-773	74LS163	A27,44,46,54,55	5	5	5	5
53	589-370	74LS165	A35	1	1	1	1
54	587-770	74LS174	A1	1	1	1	1
55	587-766	74LS191	A4-7,18-21	8	5	5	5
56	589-397	74S225 ⚠1	A17,25	2	2	2	2
57	589-449	74LS244	A36,57	2	2	2	2
58	583-331	74LS273	A8,10,28	3	3	3	3
59	589-747	74LS299	A9	1	1	1	1
60	589-587	74LS374	A16,24	2	2	2	2
61	590-024	M1100-6M	A32	1	1	1	1
62	590-023	MC68A02P ⚠1	A47	1	1	1	1
63	587-705	74LS670	A37,45	2	2	2	2
64	590-193	INTEGRATED CIRCUIT, 9637	A56	1	1	1	1
65							
66							
67	602-044	PLUG, SHORTING	J1,2	2	2	2	2
68	143-981	CONNECTOR, JACK	REF: J1,2	6	6	6	6
69							
70	582-165	SOCKET, I.C. 40 PIN DIP	REF:A47	1	1	1	1
71	582-159	24 PIN DIP	REF:A40	1	1	1	1
72	582-153	20 PIN DIP	REF:A2,3,8-10,12-17, 24,25,28,36,57	16	16	16	16
73	582-134	16 PIN DIP	REF:A1,4-7,11,18-22,27,29, 35,37,39,41,44-46,54,55	22	22	22	22
74	582-133	14 PIN DIP	REF:A23,26,30-34,38, 42,43,48-53	16	16	16	16
75	582-141	SOCKET, I.C. 8 PIN DIP	REF:A56	1	1		1
76							
77	122-494	SWITCH, ROTARY	S3,4	2	2	2	2
78	119-723	SWITCH, TOGGLE, SPDT (ON)OFF(ON)	S1,2	2	2	2	2
79	119-724	SWITCH, TOGGLE, SPDT (ON)NONE(ON)	S5	1	1		1
80		SLEEVING, SHRINK, CLEAR	REF:FL1	A/R	A/R	A/R	A/R
81	187-361	TEST LUG	TP1-9	9	9	9	9
82		NOTE: ⚠1 STATIC SENSITIVE. SPECIAL HANDLING REQUIRED PER HE1-1.					



Assembly No. 1400163. Time Code Reader/Generator PWA



NOTES: UNLESS OTHERWISE SPECIFIED –

1. RESISTORS ARE IN OHMS, 1/4 W, 5%
2. CAPACITORS ARE IN MICROFARADS
3. SCHEMATIC REFLECTS PWA 1400163-04.
4. DIODES ARE P/N 013-650

IC LIST

REF DESIG	A31	A33	A23,26,43,48,49	A22	A35	A17,25	A9	A47
AMPEX P/N	587-510	587-902	587-387	587-950	589-370	589-397	589-747	590-023
VENDOR P/N	74LS00	74LS05	74LS74	74LS151	74LS165	74S225	74LS299	MC68A02P
VOLTAGE (PIN)	+5V (14)	+5V (14)	+5V (14)	+5V (16)	+5V (16)	+5V (20)	+5V (20)	+5V (8)
GROUND (PIN)	(7)	(7)	(7)	(8)	(8)	(10)		(1,21)
REF DESIG	A51	A42	A34	A11	A1	A36,57	A16,24	A37,45
AMPEX P/N	587-750	587-534	587-746	587-760	587-770	589-449	589-537	587-705
VENDOR P/N	74LS02	74LS08	74LS86	74LS157	74LS174	74LS244	74LS374	74LS670
VOLTAGE (PIN)	+5V (14)	+5V (14)	+5V (14)	+5V (16)	+5V (16)	+5V (20)	+5V (20)	+5V (16)
GROUND (PIN)	(7)	(7)	(7)	(8)	(8)	(10)	(10)	(8)
REF DESIG	A38,50,53	A30,52	A39	A27,44,46,54,55	A4-7, 18-21	A8,10,28	A32	A56
AMPEX P/N	587-533	587-523	587-279	587-773	587-766	589-331	589-905	590-193-
VENDOR P/N	74LS04	74LS32	74LS138	74LS163	74LS191	74LS273	M1100-6M	9637
VOLTAGE (PIN)	+5V (14)	+5V (14)	+5V (16)	+5V (16)	+5V (16)	+5V (20)	+5V (14)	+5V (8)
GROUND (PIN)	(7)	(7)	(8)	(8)	(8)	(10)	(7)	(4)

PROM LIST

REF DESIG	A40	A14	A12	A2	A29
AMPEX P/N	1400300-06	1400302-01	1400304-01	1400306-01	1400308-01
VENDOR P/N	—	—	—	—	—
VOLTAGE (PIN)	+5V (24)	+5V (20)	+5V (20)	+5V (20)	+5V (16)
GROUND (PIN)	(12)	(10)	(10)	(10)	(8)
REF DESIG	A15	A13	A3	A41	
AMPEX P/N	1400301-01	1400303-01	1400305-01	1400307-01	
VENDOR P/N	—	—	—	—	
VOLTAGE (PIN)	+5V (20)	+5V (20)	+5V (20)	+5V (16)	
GROUND (PIN)	(10)	(10)	(10)	(8)	

REFERENCE DESIG

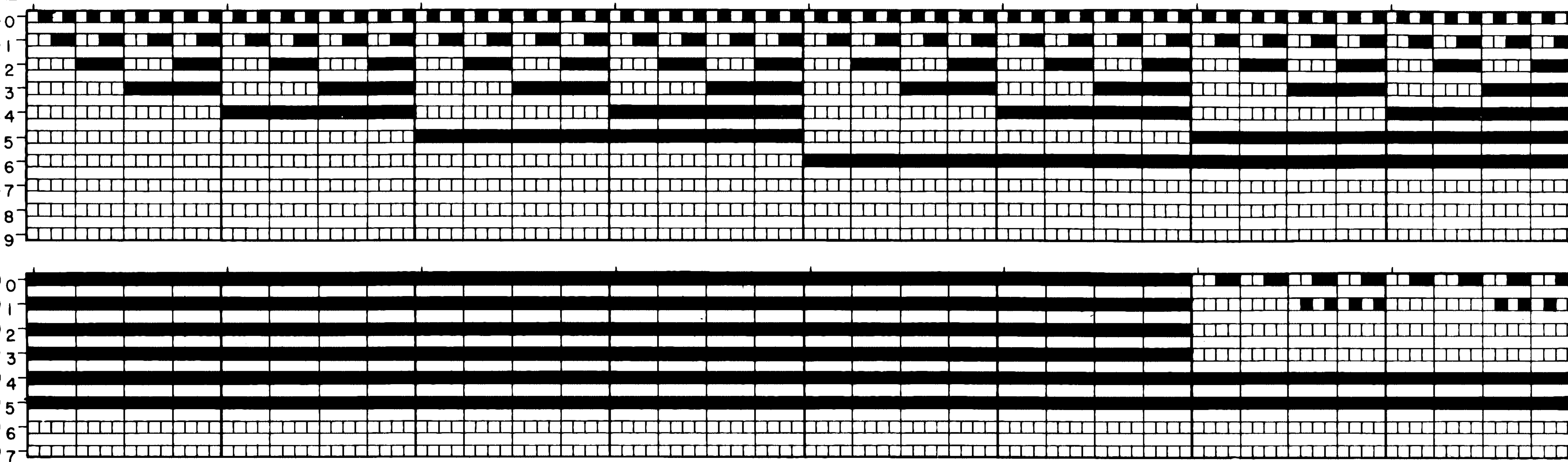
LAST USED	NOT USED
A57 C34 FL1 J2 R17 RN2 S5 TP9 CR3	

Schematic No. 1400165D. Time Code Reader/Generator

PROM CODING CHART

ADDRESS:
HEX 000 010 020 030 040 050 060 070
DECIMAL 0 016 032 048 064 080 096 112

INPUT ADDRESS
A0 B1 PHASE TC
A1 B1 Ø TC IN
A2 B1 Ø TC FB
A3 NRZ TC FB
A4 NRZ CLK FB
A5 ENABLE
A6 LOAD 1
A7 LOAD 2
A8
A9

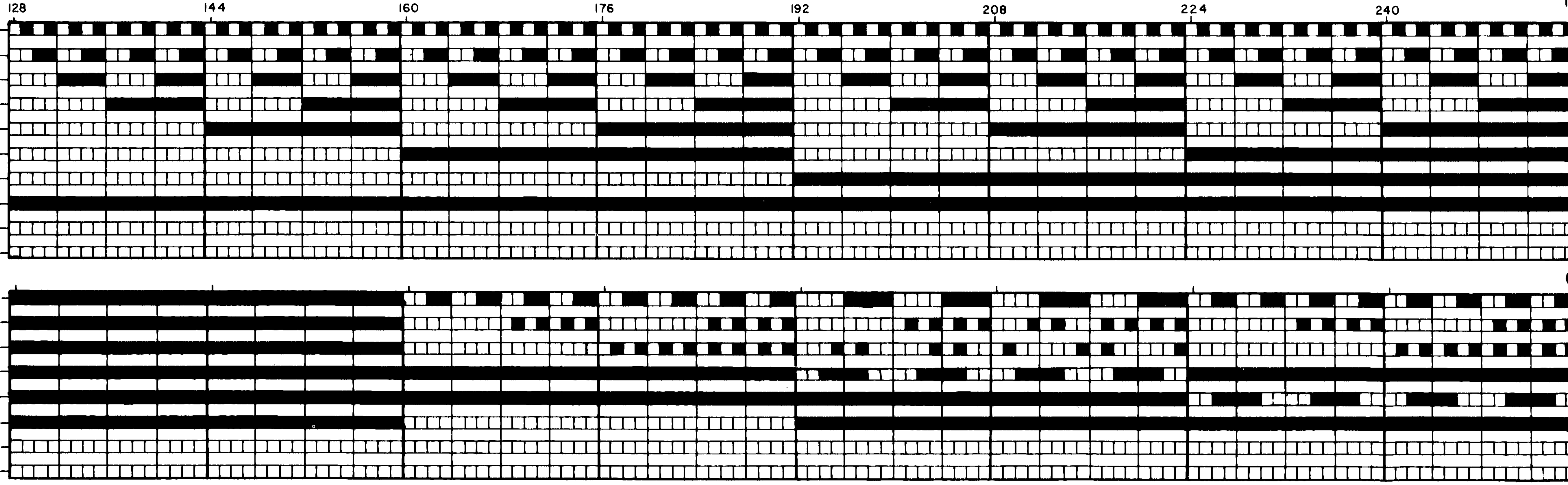


OUTPUT DATA
D0 BI Ø TC
D1 NRZ TC
D2 NRZ CLK
D3 ENABLE
D4 LOAD 1
D5 LOAD 2
D6
D7

FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF00110011021302130415041506170617 HEX D_0-D_3
33333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333333 HEX D_4-D_7

HEX 080 090 0A0 0B0 0C0 0D0 0E0 0F0
DECIMAL 128 144 160 176 192 208 224 240

INPUT ADDRESS
A0 B1 PHASE TC
A1 B1 Ø TC IN
A2 B1 Ø TC FB
A3 NRZ TC FB
A4 NRZ CLK FB
A5 ENABLE
A6 LOAD 1
A7 LOAD 2
A8
A9



OUTPUT DATA
D0 BI Ø TC
D1 NRZ TC
D2 NRZ CLK
D3 ENABLE
D4 LOAD 1
D5 LOAD 2
D6
D7

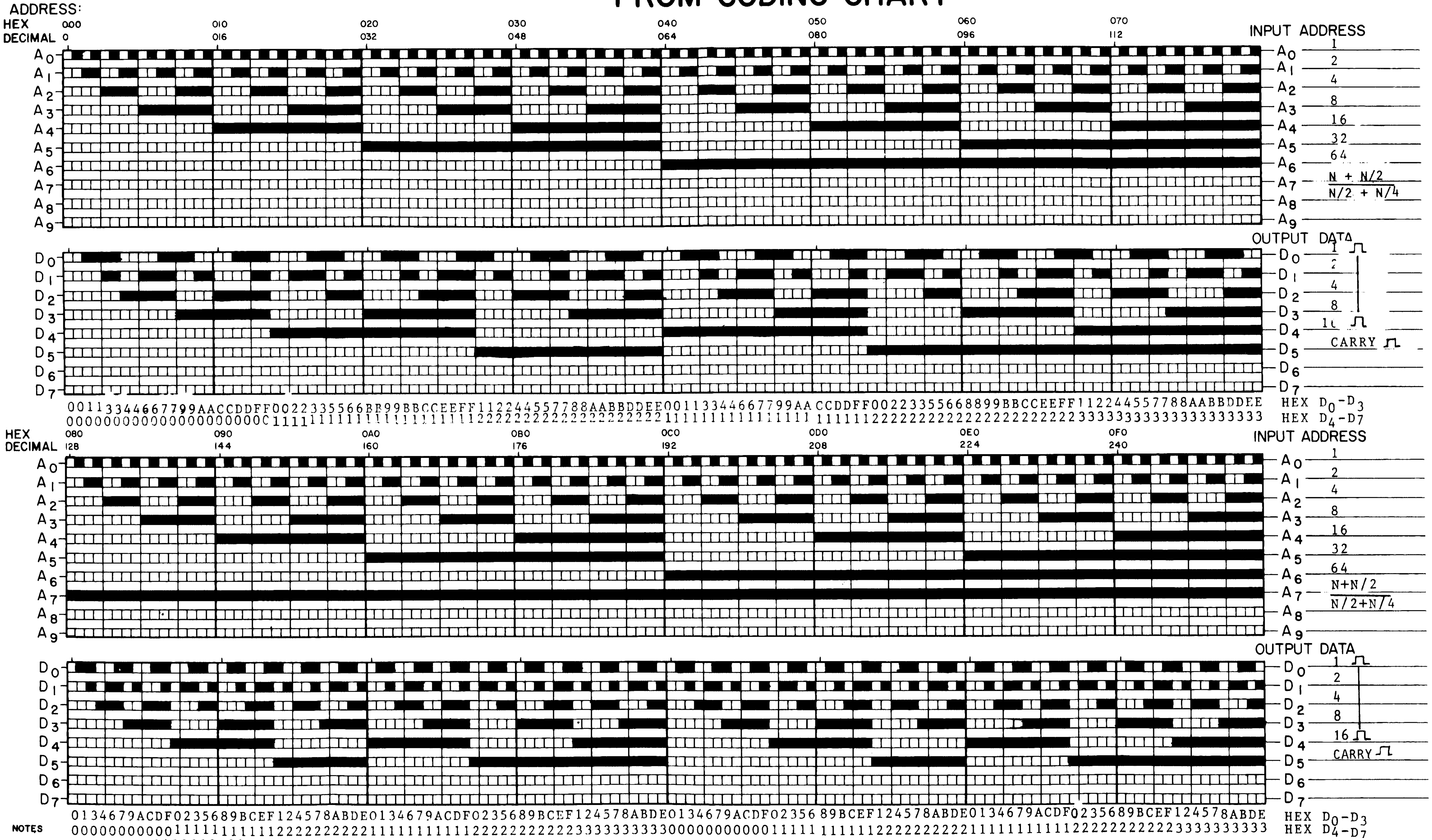
FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF889988998A9B8A9B8C9D8C9B8E9F8E9F008C9D11028E9F13048A9B15068A9B17889988998A9B8A9B8C9D8C9D8E9F8E9F HEX D_0-D_3
33333333333333333333333333333333111111111111111111111111111111113333333333333333333333333333333322333322233332223333322223333322 HEX D_4-D_7

NOTES

1. PROM PART NO. IS 1400301-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400301
4. PAPER TAPE PT 1400301-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS 922902

PROM No. 1400301. B1 ϕ Decoder Control PROM, A15

PROM CODING CHART

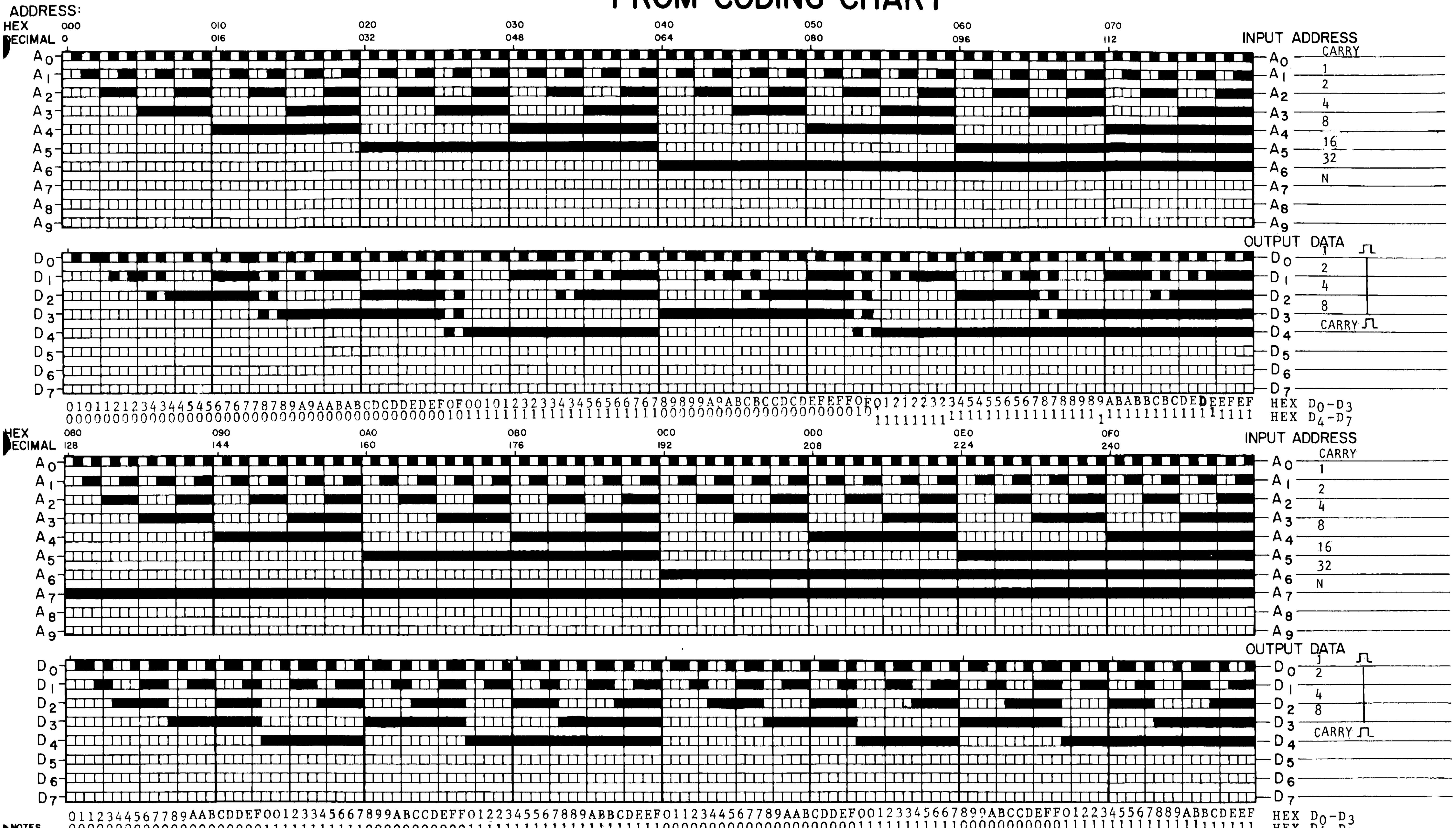


NOTES

1. PROM PART NO. IS 1400302-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400302
4. PAPER TAPE PT 1400302-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS 8H5542

PROM No. 1400302. B1 ϕ Decoder 1
PROM, A14

PROM CODING CHART

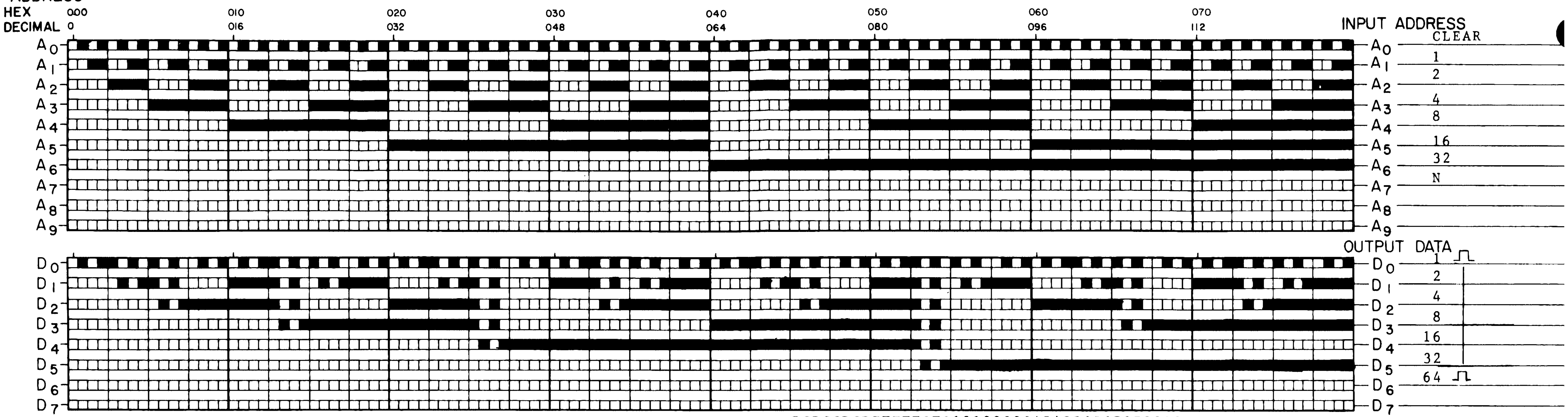


NOTES

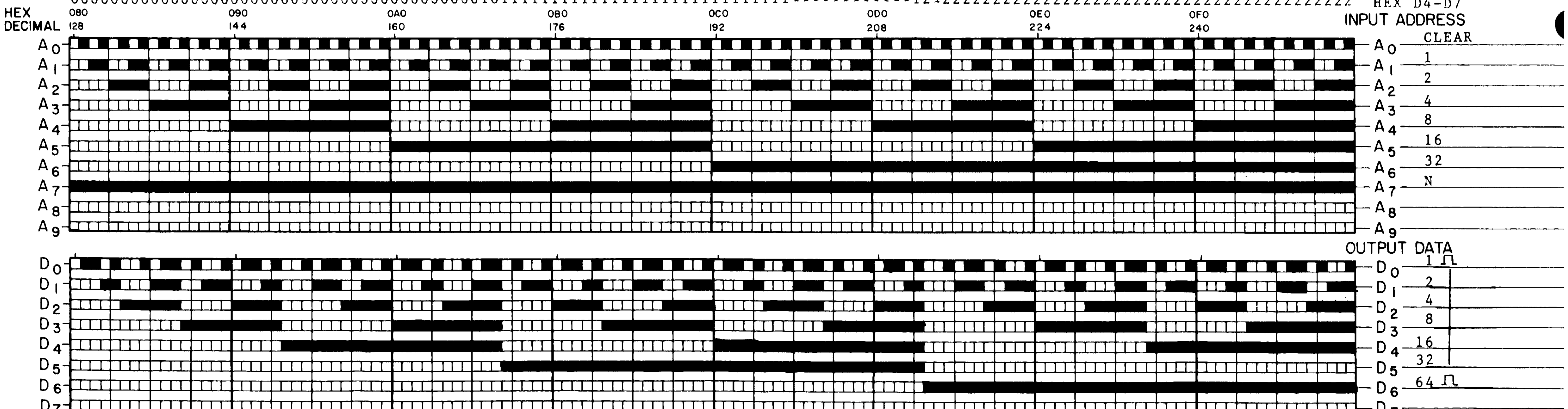
1. PROM PART NO. IS 1400303-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400303
4. PAPER TAPE PT 1400303-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS —9HL23.

PROM No. 1400303. B1 ϕ Decoder 2
PROM, A13

PROM CODING CHART



0101121234344545676778789A9AABABCDCDDEDEF0F00101232334345656676789899A9ABCBCCDCDEFEFF0F012122323454556565678788989ABABBCBCDEDEEFEF HEX D0-D3
0000000000000000000000000000000000000000000000101111111111111111111111111111111111111111111111121222222222222222222222222222222222 HEX D4-D7



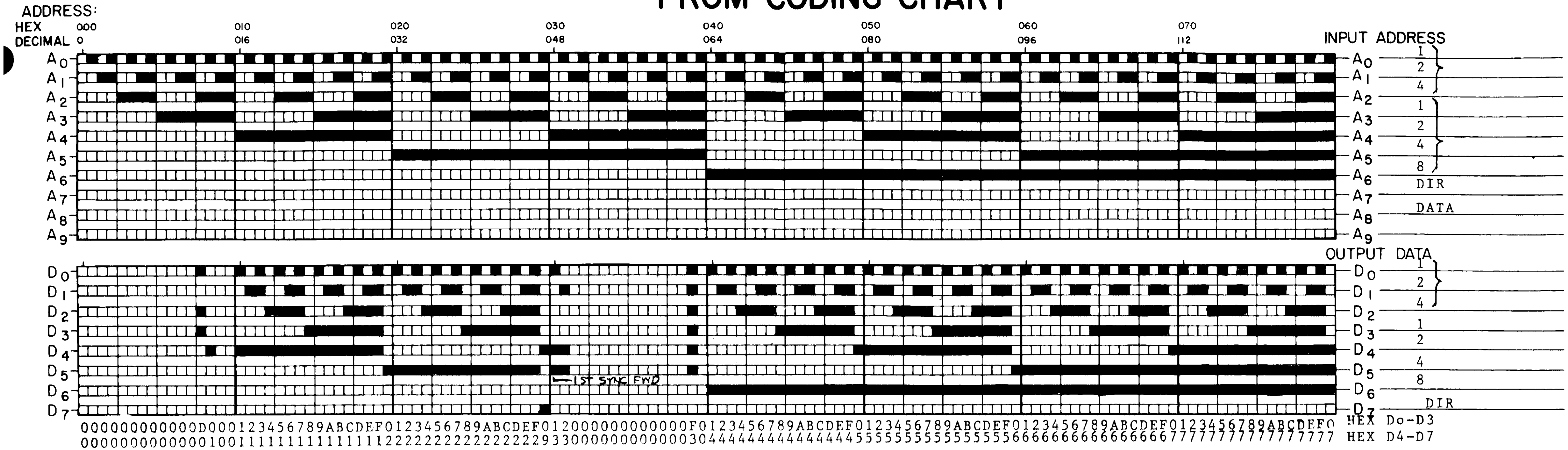
0112344567789AABCDDEF0012334566789 9ABCCDEFF0122345567889ABBCDEEF0112344567789AABCDDEF0012334566789 9ABCCDEFF0122345567889ABBCDEEF HEX Do-D3
00000000000000000000011111111111111111111112222222222222222222222222222333333333333333333333333334444444444444444444444444445555555555555555555555 HEX D4-D7

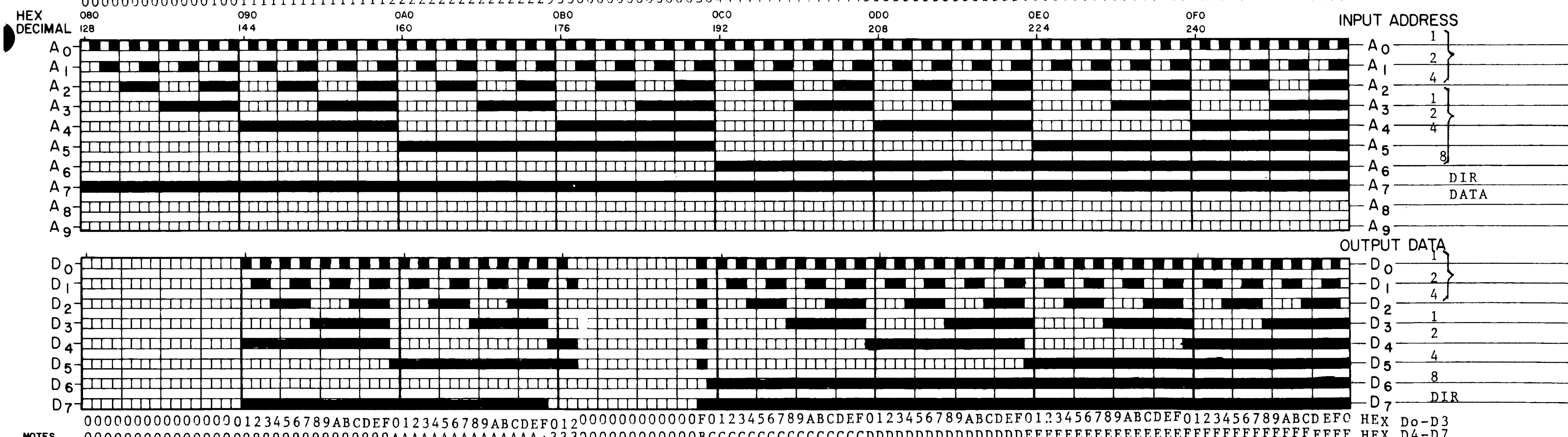
NOTES

1. PROM PART NO. IS 1400304-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400304
4. PAPER TAPE PT 1400304-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS 5547A7

PROM No. 1400304. B1 ϕ Decoder 3
PROM, A12

PROM CODING CHART



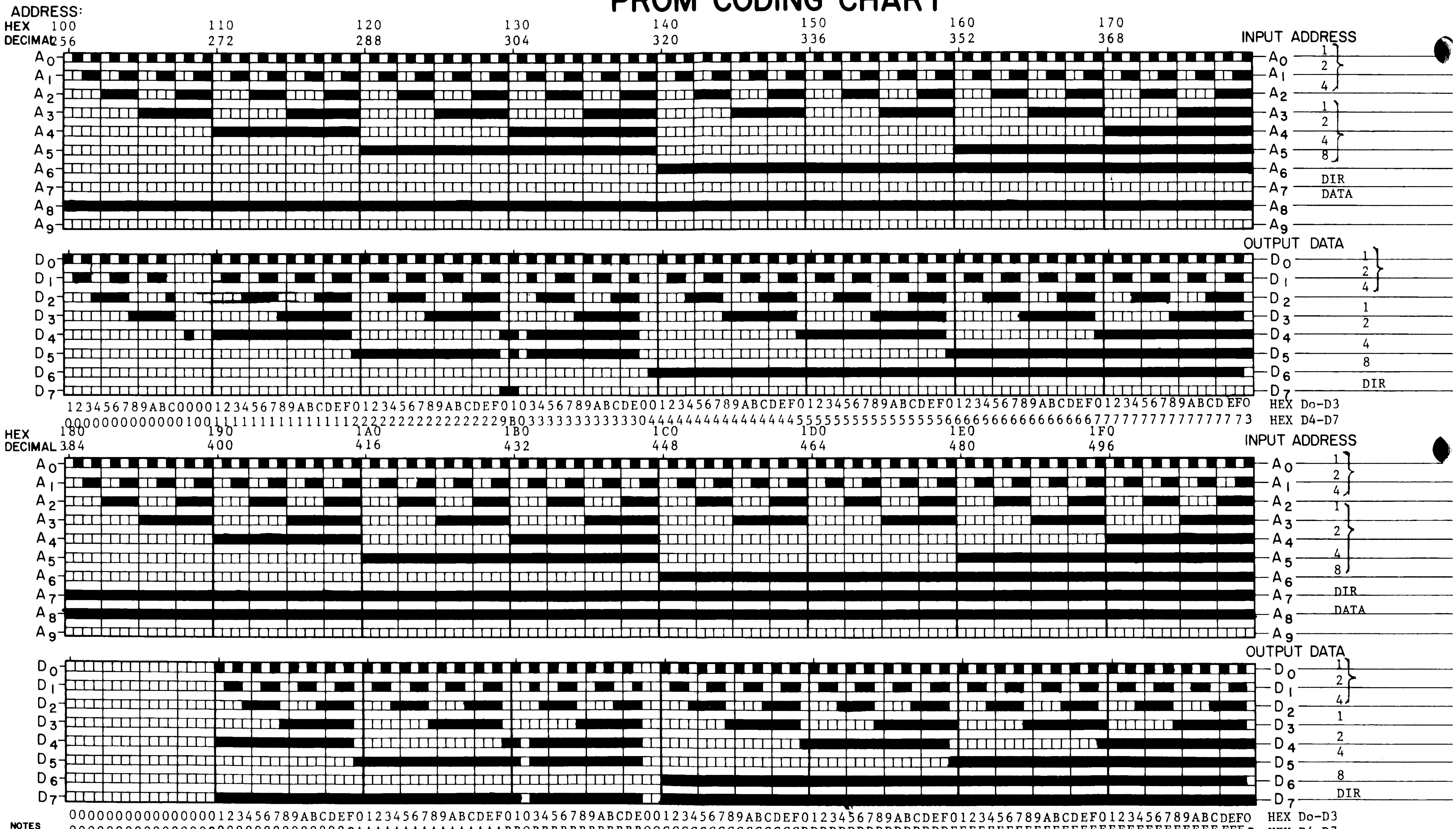


NOTES

1. PROM PART NO. IS 1400305-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400305
4. PAPER TAPE PT 1400305-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS 42L__6P

PROM No. 1400305. Sync Detector PROM, A3 (Sheet 1 of 2)

PROM CODING CHART

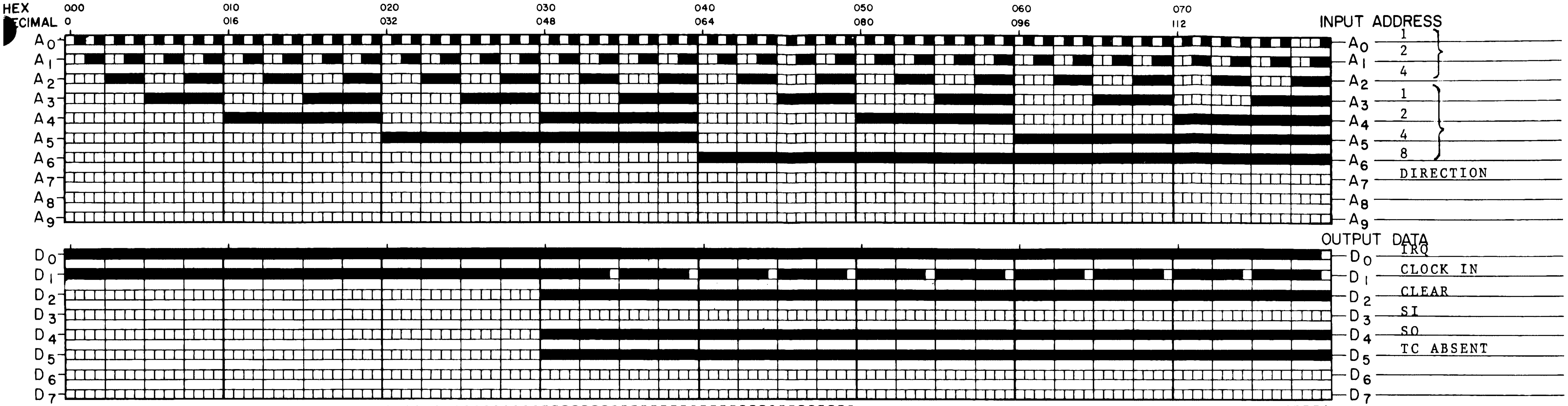


NOTES

1. PROM PART NO. IS
2. MAKE FROM AMPEX PART NO.
3. PROGRAM AND MARK PER SC
4. PAPER TAPE PT
   AVAILABLE FROM AVSD DOCUMENT CONTROL.

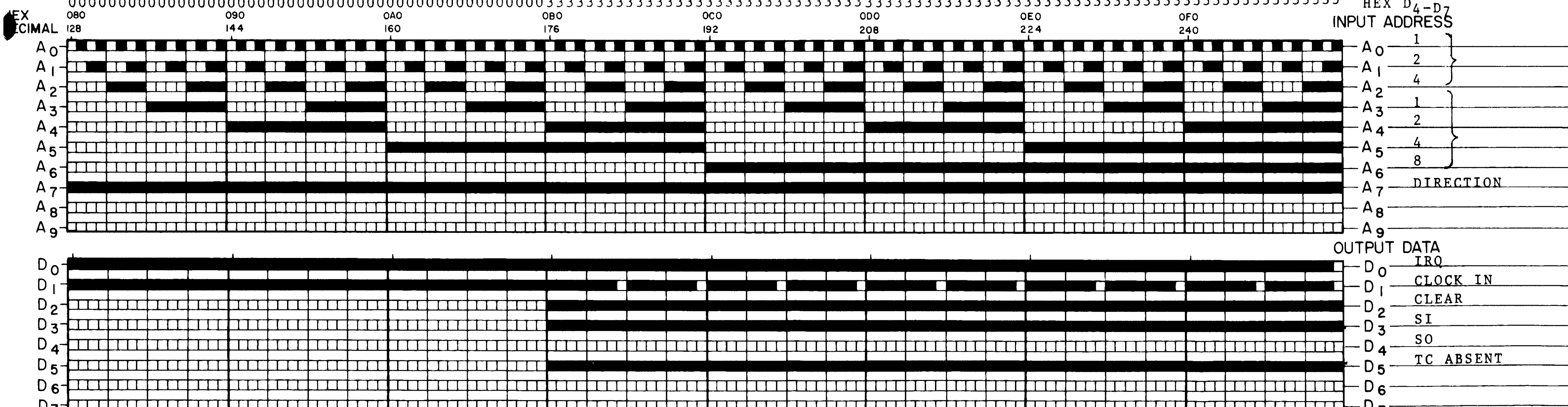
PROM No. 1400305. Sync Detector
PROM, A3 (Sheet 2 of 2)

PROM CODING CHART



333333333333333333333333333333333333333333333333777777757777777577777775777777757777777577777775777777757777777577777775777777774 HEX D_0-D_3

00000000000000000000000000000000000000000000000033333333333333333333333333333333333333333333333333333333333333333333333333333333 HEX D_4-D_7



333333333333333333333333333333333333333333333333FFFFFFFDFFFFFFFDFFFFFFFDFFFFFFFDFFFFFFFDFFFFFFFDFFFFFFFDFFFFFFFDFFFFFFFDFFFFFFFC HEX D_0-D_3

00000000000000000000000000000000000000000000000022222222222222222222222222222222222222222222222222222222222222222222222222222222 HEX D_4-D_7

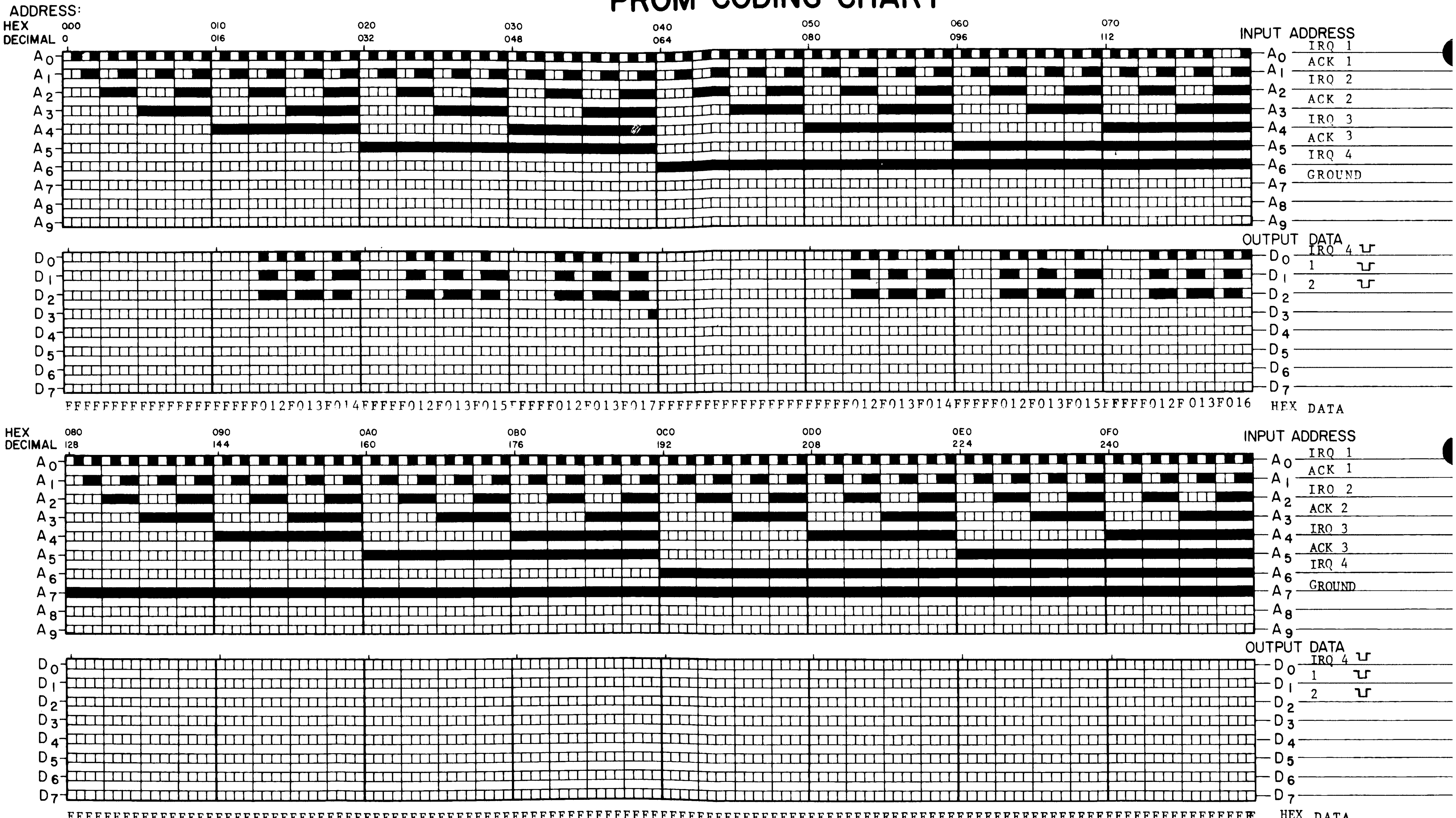
NOTES

1. PROM PART NO. IS 1400306-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400306
4. PAPER TAPE PT 1400306-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS 2AP5LP

PROM No. 1400306. FIFO
Control PROM, A2

AMPEX 1809449-03

PROM CODING CHART

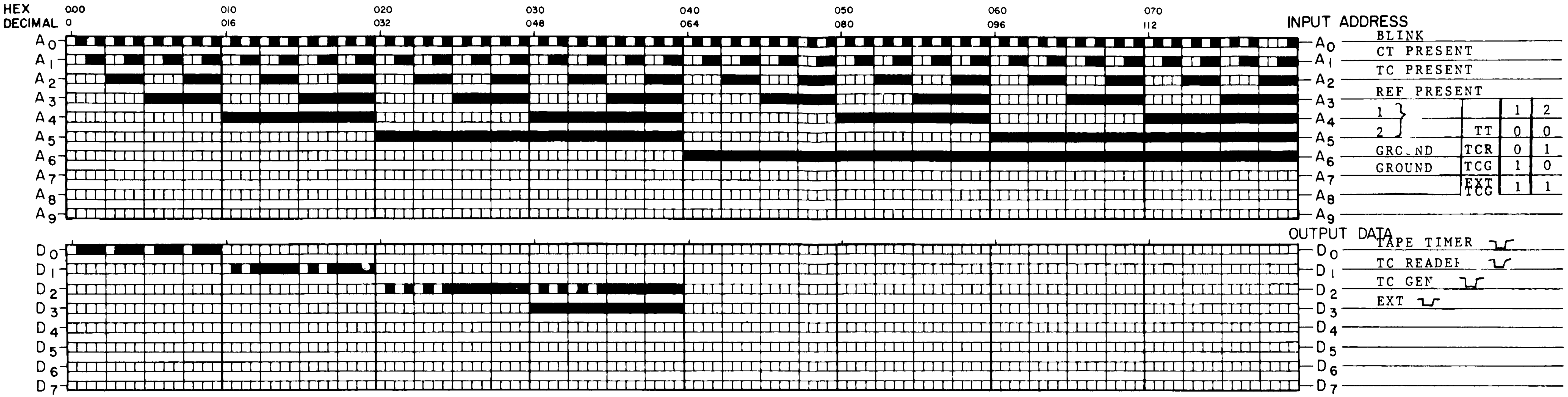


NOTES

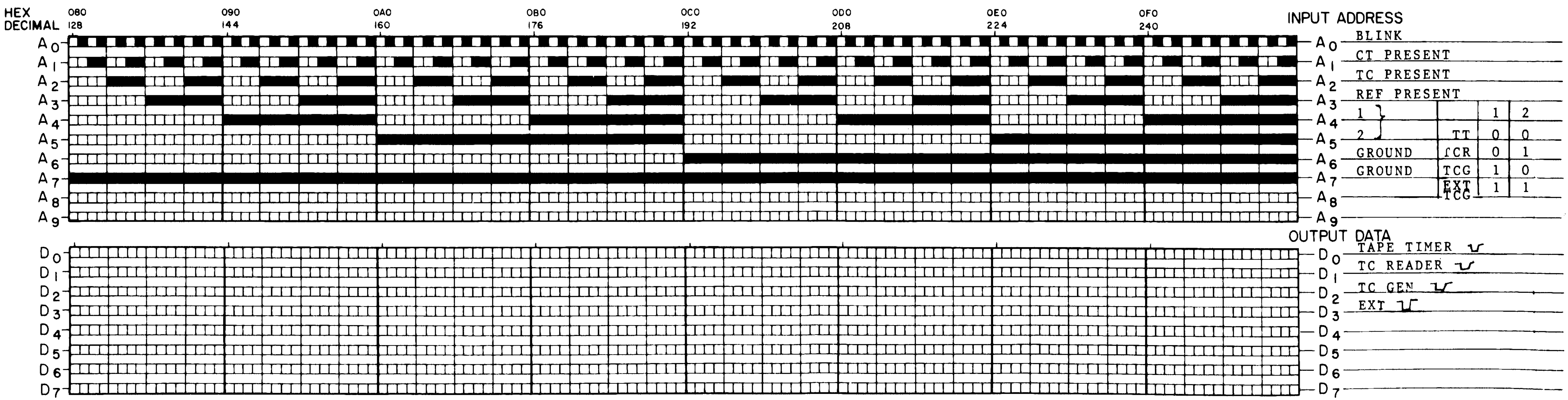
1. PROM PART NO. IS 1400307-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400307
4. PAPER TAPE PT 1400307-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS AP17P6
6. ■ INDICATES A DATA OUTPUT 0.

PROM No. 1400307. Interrupt Control PROM, A41

PROM CODING CHART



FEEEFEEEFEEEFEEEFDFDDDDDFDFDDDDDFBFBFBFBBBBBBBBB7373737333333333FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF HEX DATA



FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF HEX DATA

NOTES

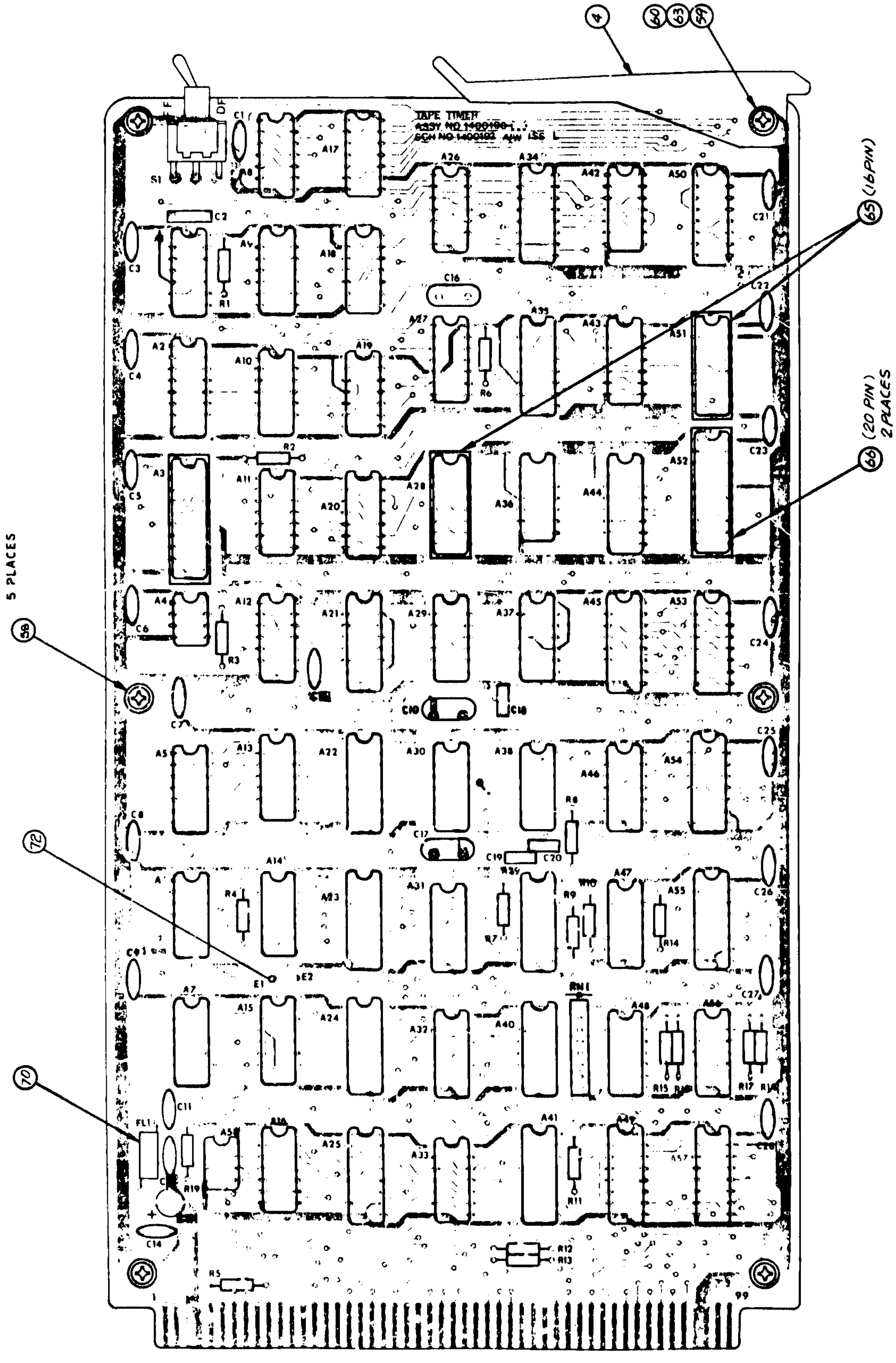
1. PROM PART NO. IS 1400308-01
2. MAKE FROM AMPEX PART NO. 589-676
3. PROGRAM AND MARK PER SC 1400308
4. PAPER TAPE PT 1400308-01 AVAILABLE FROM AVSD DOCUMENT CONTROL.
5. PROM SIGNATURE IS L68A6A
6. ■ INDICATES AN OUTPUT DATA 0.

PROM No. 1400308. Mode Display Control PROM, A29

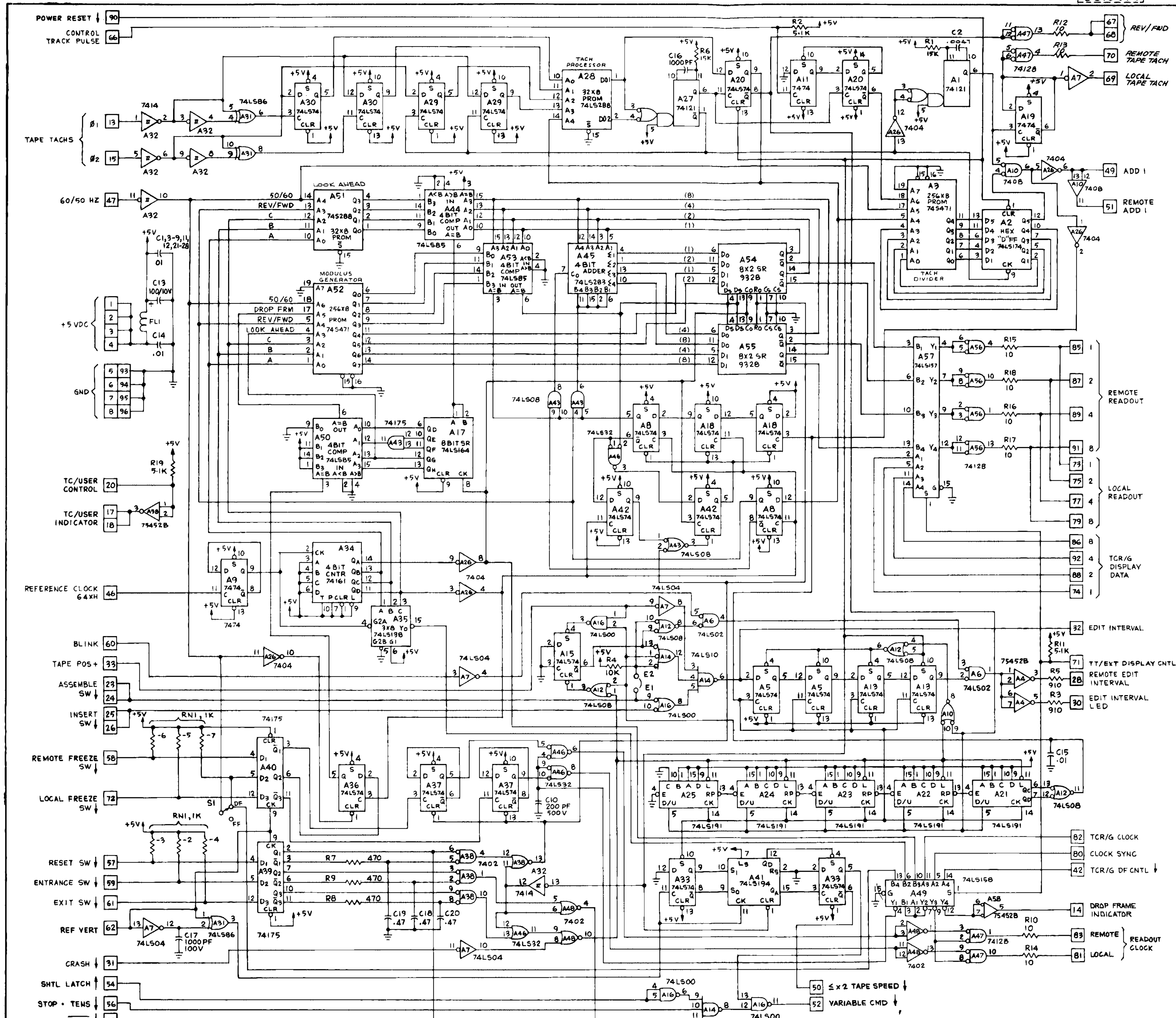
ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	-05	-06	-07
1				-07	-07	
2	1400192	SCHEMATIC TAPE TIMER		F	G	J
3	1400003-01	SHIELD		1	1	1
4	1400004-01	HANDLE		1	1	1
5	1400005-AV	LABEL		1	1	1
6						
7	1400337	PROM TACH PROCESSOR	A28	-01	-01	-01
8	1400338	PROM TACH DIVIDER	A3	-01	-01	-01
9	1400339	PROM LOOK AHEAD	A51	-01	-01	-01
10	1400340	PROM MODULUS GENERATOR	A52	-01	-01	-01
11						
12	1374188-01	INDUCTOR FILTER	FL1	1	1	1
13	035-734	CAPACITOR, MYLAR, .01uF, 50V	C2	1	-	-
14	034-286	CAPACITOR, MICA, 200pF, 500V	C10	1	1	1
15	034-950	CAPACITOR, MICA, 1000pF, 100V	C16,17	2	2	2
16	037-894	CAPACITOR, TANT, 100uF, 10V	C13	1	1	1
17	064-116	CAPACITOR, CER., DISC, .01, 50V	C1,3-9,11,12,14,15, 21-28	20	20	20
18	064-309	CAPACITOR, CER., MONO, .47, 100V	C18,19,20	3	3	3
19	035-730	CAPACITOR, MYLAR, .0047uF, 50V	C2	-	1	1
20	066-810	RESISTOR, FIXED, C.F., 10 OHMS, 1/4W, 5%	R10,12-18	8	8	8
21	066-818	RESISTOR, FIXED, C.F., 470 OHMS, 1/4W, 5%	R7,8,9	3	[illegible]	3
22	066-822	RESISTOR, FIXED, C.F., 910 OHMS, 1/4W, 5%	R3,5	2	2	2
23	066-830	RESISTOR, FIXED, C.F., 10K OHMS, 1/4W, 5%	R4	1	1	1
24	066-842	RESISTOR, FIXED, C.F., 5.1K OHMS, 1/4W, 5%	R2,11,19	3	3	3
25	066-856	RESISTOR, FIXED, C.F., 15K OHMS, 1/4W, 5%	R1,6	2	2	2
26	039-223	RESISTOR NETWORK, 1K OHMS	RN1	1	1	1
27						
28	587-510	INTEGRATED CIRCUIT, 74LS00	A16		1	1
29	586-109	7402	A38,48	2	2	2
30	587-750	74LS02	A6	1	1	1
31	586-326	7404	A26	1	1	-
32	587-533	74LS04	A7	1	1	-
33	586-759	7408	A10	1	1	1
34	587-534	74LS08	A12,43	2	2	2
35	587-283	74LS10	A14	1	1	1
36	587-147	7414	A32	1	1	1
37	586-326	INTEGRATED CIRCUIT, 7404	A7,26	-	-	2

AMPEX	Ampex Corporation REDWOOD CITY, CALIFORNIA	CODE IDENT NO 92739	LIST OF MATERIALS	LM-1400190 SHEET 2	V

ITEM NO	PART NUMBER	DESCRIPTION	REF DESIG	-05	-06	-07
38						
39	587-523	INTEGRATED CIRCUIT, 74LS32	A46	1	1	1
40	586-108	7474	A9,11,19	3	3	3
41	587-387	74LS74	A5,8,13,15,18,20,29,30, 33,36,37,42	12	12	12
42	587-755	74LS85	A44,50,53	3	3	3
43	587-746	74LS86	A31	1	1	1
44	586-533	74121	A1,27	2	2	2
45	587-479	74128	A47,56	2	2	2
46	587-279	74LS138	A35	1	1	1
47	587-760	74LS157	A57	1	1	1
48	589-089	74LS158	A49	1	1	1
49	586-922	74161	A34	1	1	1
50	587-895	74LS164	A17	1	1	1
51	587-770	74LS174	A2	1	1	1
52	586-925	74175	A39,40	2	2	2
53	587-766	74LS191	A21-25	5	5	5
54	589-091	74LS194	A41	1	1	1
55	587-814	74LS283	A45	1	1	1
56	587-493	75452B	A4,58	2	2	2
57	589-108	INTEGRATED CIRCUIT, 9328	A54,55	2	2	2
58	474-500	SCREW, MACH, PAN HD, XREC, 4-40x.312 LG				5
59	283-105	SPACER, PLAIN, .140 I.D., X .250 O.D., X .125 LG		1	1	1
60	471-063	SCREW, PAN HD., 4-40 X .438 LG		1	1	1
61	473-325	SCREW, PAN HD., ASSEM. WASH. 4-40 X .312 LG		5	5	—
62	501-169	WASHER, SMALL PATTERN, PLAIN #4		5	5	—
63	502-002	WASHER, SPLIT LOCK, #4		1	1	1
64	506-011	WASHER, BOWED		1	1	1
65	582-134	SOCKET, 16 PIN DIP	REF: A28,51	2	2	2
66	582-153	SOCKET, 20 PIN DIP	REF: A3,52	2	2	2
67						
68						
69	120-967	SWITCH	S1	1	1	1
70		SLEEVING, SHRINK, CLEAR	REF: FL1	-	-	A/R
72	615-004	WIRE, SOLID, UNINSULATED, 24 AWG				A/R



Assembly No. 1400192. Tape Timer PWA



NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE IN OHMS, 1/4 W, 5 %
2. CAPACITORS ARE IN MICROFARADS
3. THIS SCHEMATIC REFLECTS PWA 1400190-07.

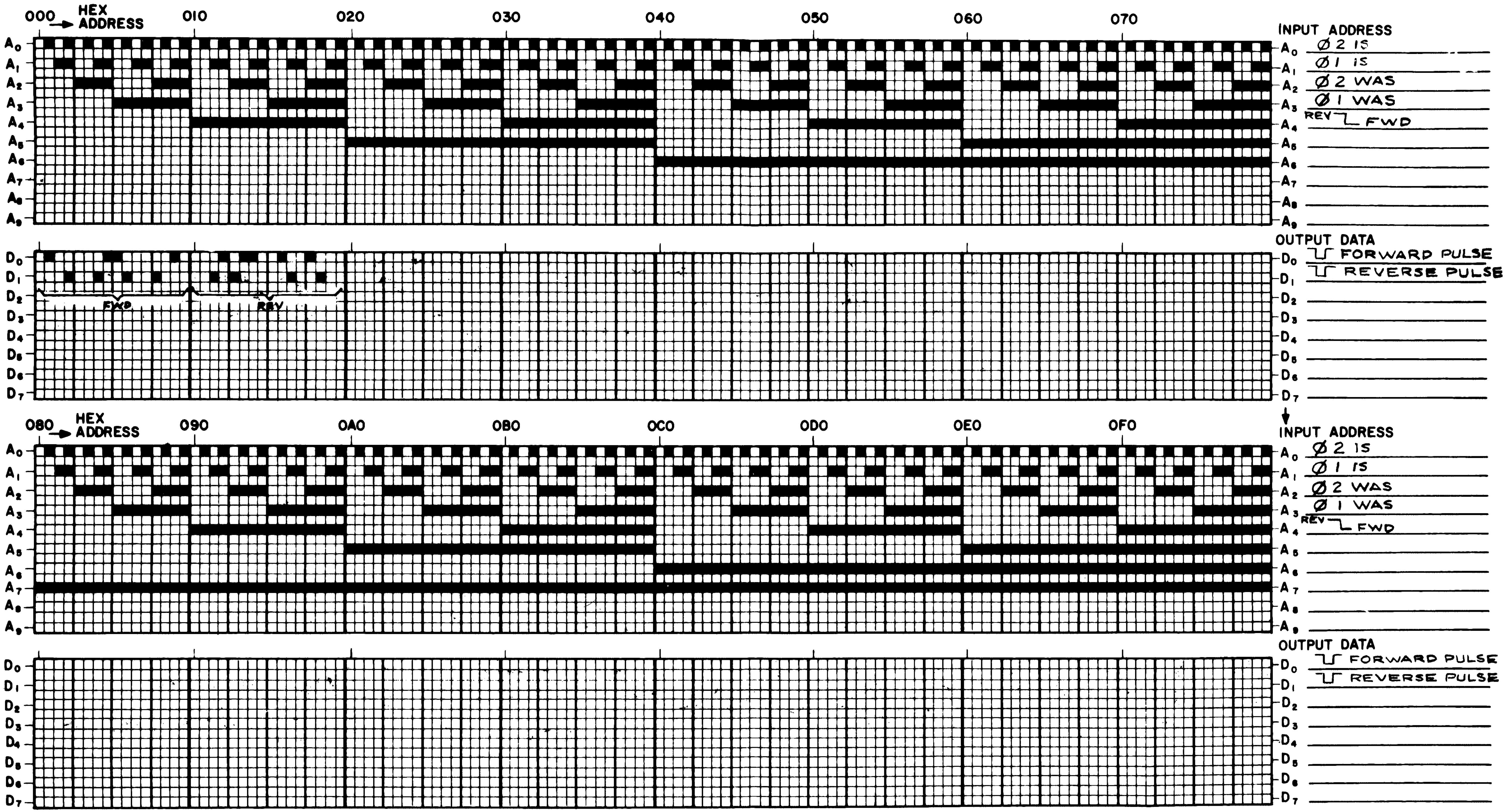
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A58 C28 E2 FL1 R19 RN1 S1	

I. C. LIST

REFERENCE DESIGNATION	A16	A26,7	A12,43	A46	A44,50,53	A47,56	A49	A2	A41	A54,55	A51
AMPEX P/N	587-510	586-326	587-534	587-523	587-755	587-479	589-089	587-770	589-091	589-108	1400339-01
VENDOR P/N	74LS00	7404	74LS08	74LS32	74LS85	74128	74LS158	74LS174	74LS194	9328	—
VOLTAGE PIN	14	14	14	14	16	14	16	16	16	16	16
GROUND PIN	7	7	7	7	8	7	8	8	8	8	8
REFERENCE DESIGNATION	A38,48		A14	A9,11,19	A31	A35	A34	A39,40	A45	A28	A52
AMPEX P/N	586-109		587-283	586-108	587-746	587-279	586-922	586-925	587-814	1400337-01	1400340-01
VENDOR P/N	7402		74LS10	7474	74LS86	74LS138	74161	74175	74LS283	—	—
VOLTAGE PIN	14		14	14	14	16	16	16	16	16	20
GROUND PIN	7		7	7	7	8	8	8	8	8	10
REFERENCE DESIGNATION	A6	A10	A32	A5,8,13,15,18,20,29,30,33,36,37,42	A1,27	A57	A17	A21-25	A4,58	A3	
AMPEX P/N	587-750	586-759	587-147	587-387	586-533	587-760	587-895	587-766	587-493	1400338-01	
VENDOR P/N	74LS02	7408	7414	74LS74	74121	74LS157	74LS164	74LS191	75452B	—	
VOLTAGE PIN	14	14	14	14	14	16	14	16	8	20	
GROUND PIN	7	7	7	7	7	8	7	8	4	10	

Schematic No. 1400192J.
Tape Timer

PROM CODING CHART

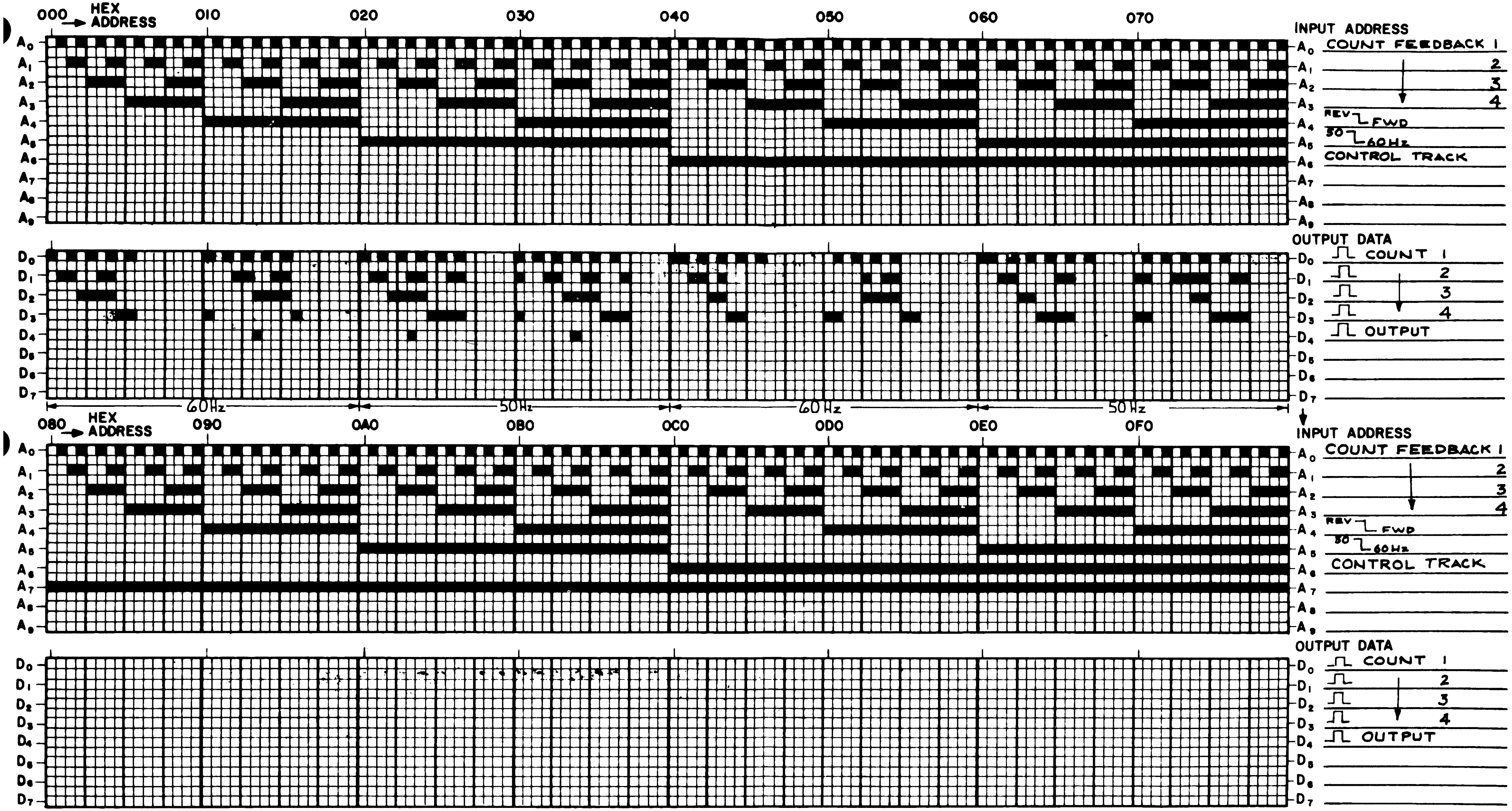


SCHEMATIC NO. 1400192
SCHEMATIC REF. NO. A28
NEXT ASSEMBLY NO. 1400190 (TAPE TIMER)
PROM NO. / PART NO. 1400337-01

AMPEX 1809449-03

PROM No. 1400337. Tach Processor PROM, A28

PROM CODING CHART



SCHEMATIC NO. 1400192

SCHEMATIC REF. NO. A3

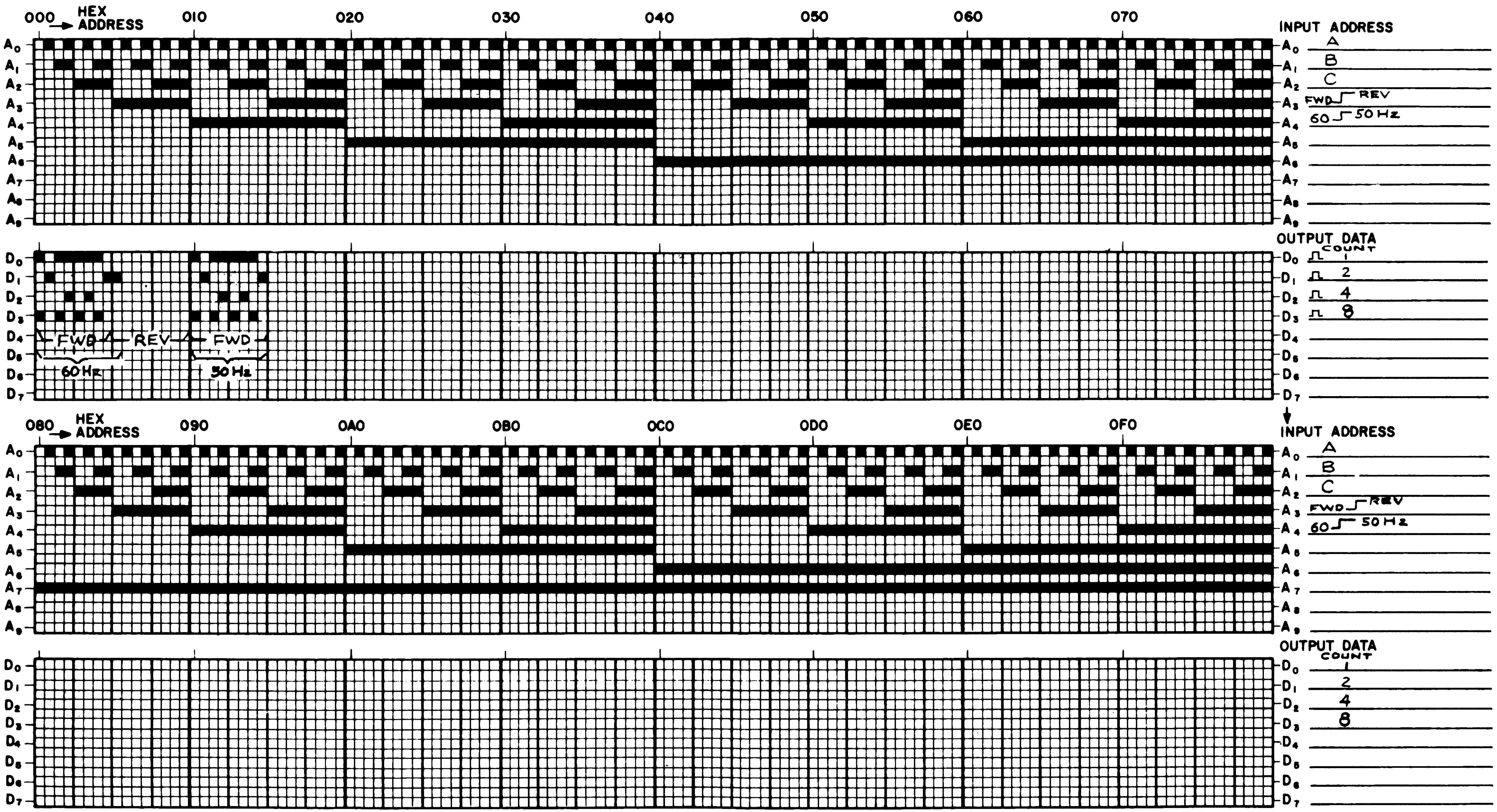
NEXT ASSEMBLY NO. 1400190

PROM NO. / PART NO. 1400338-01

AMPEX 1809449-03

PROM No. 1400338. Tach Divider PROM, A3

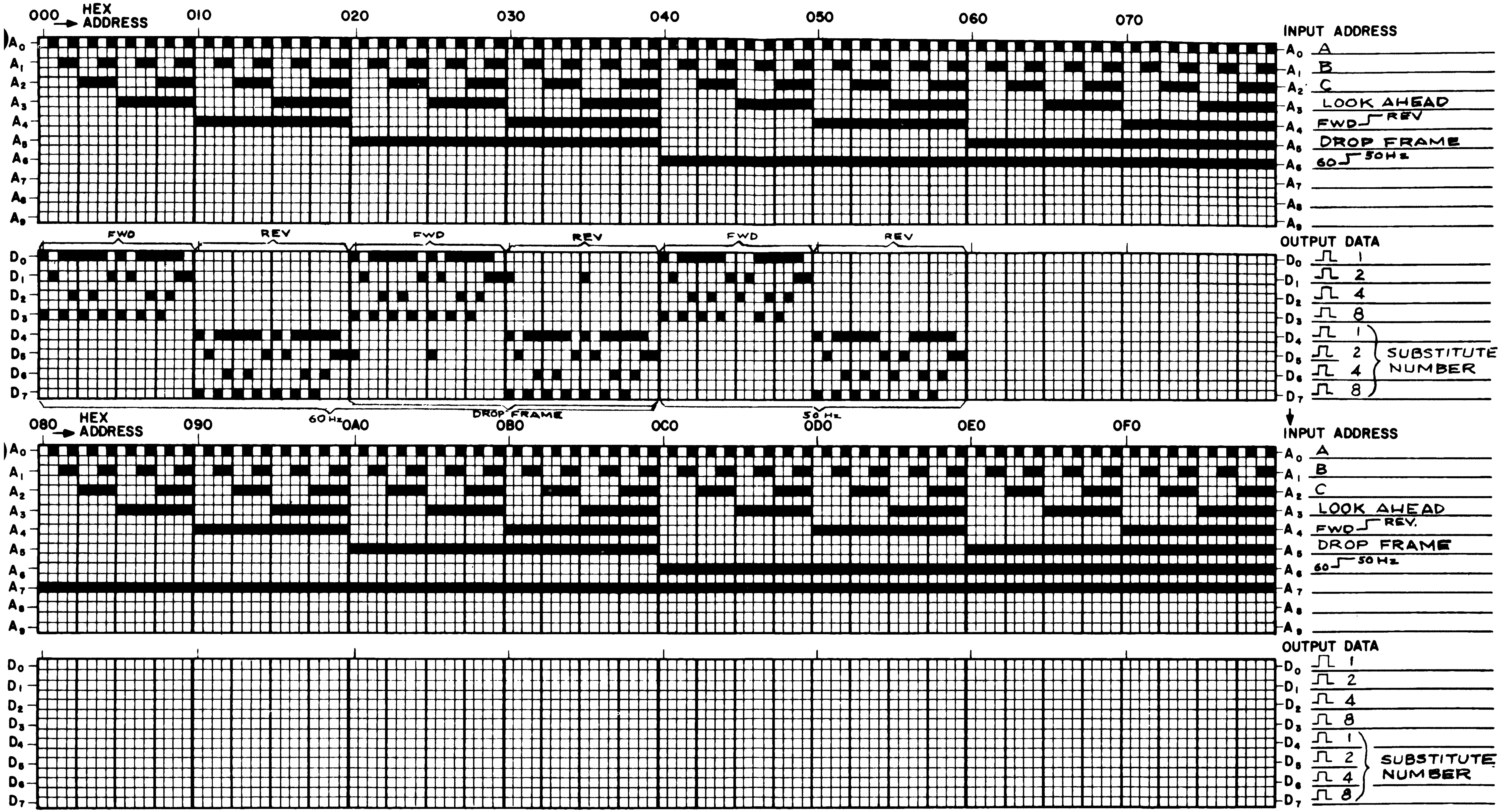
PROM CODING CHART



SCHEMATIC NO. 1400192
SCHEMATIC REF. NO. A51
NEXT ASSEMBLY NO. 1400190
PROM NO. / PART NO. 1400339-01

PROM No. 1400339. Look Ahead Prom, A51

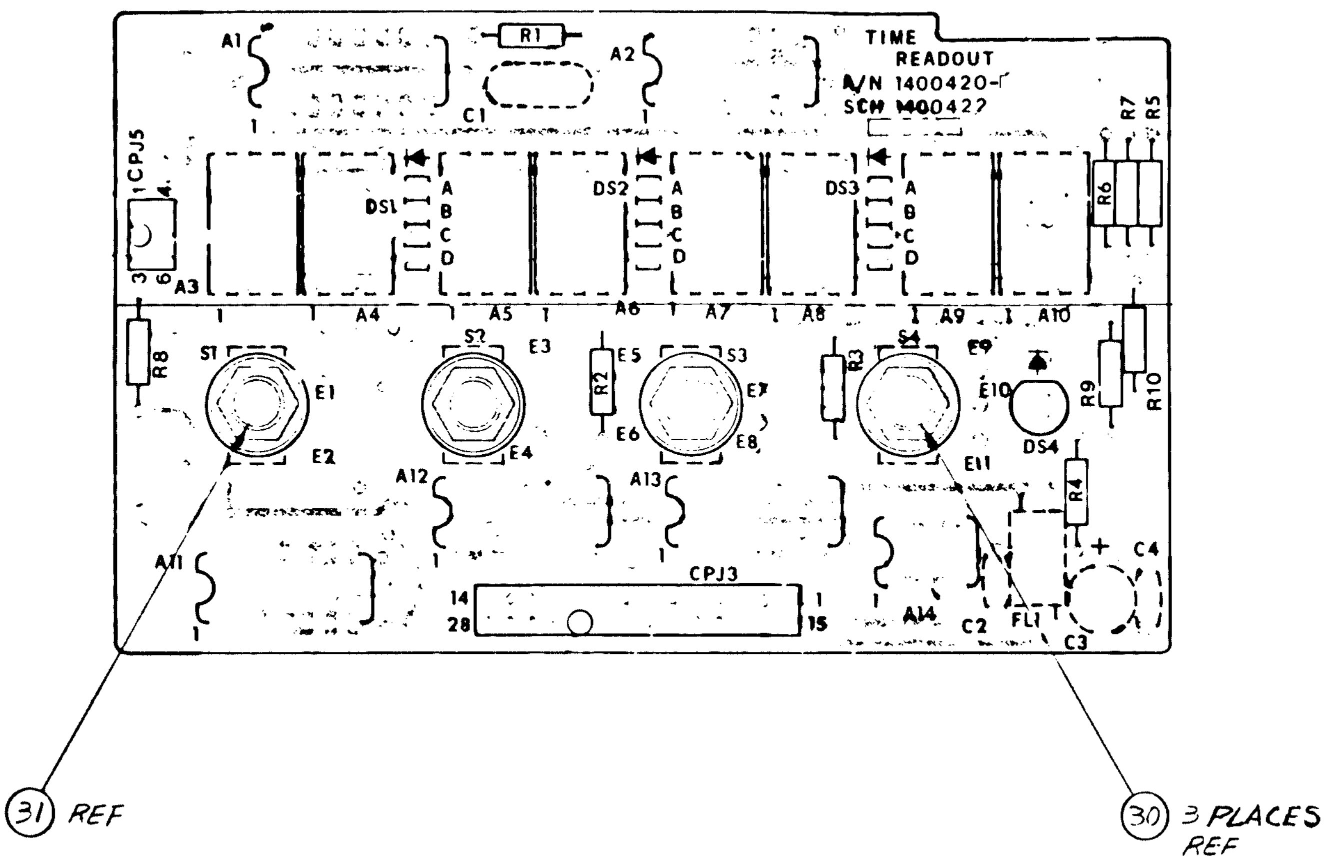
PROM CODING CHART



SCHEMATIC NO. 1400192
SCHEMATIC REF. NO. A52
NEXT ASSEMBLY NO. 1400190
PROM NO. / PART NO. 1400340-01

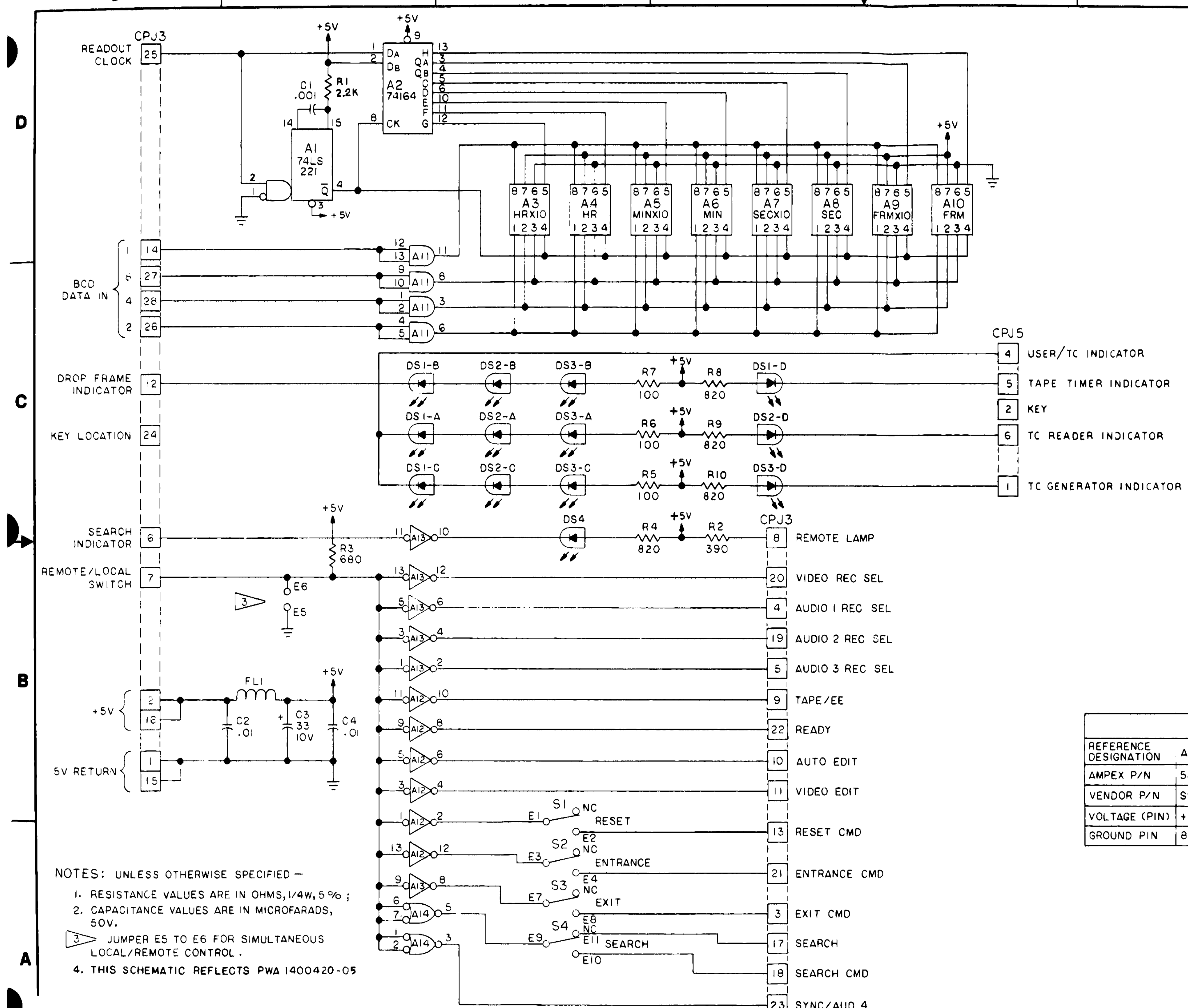
PROM No. 1400340. Modulus Generator PROM, A52

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER				
				-01	-02	-03	-04	-05
1				-01	-01	-02	-03	
2	1400422	SCHEMATIC		(-)	A	B	C	D
3	1374188-01	INDUCTOR, FILTER	FL1	1	1	1	1	1
4								
5	034-950	CAPACITOR, MICA, 1000 pF	C1	1	1	1	1	1
6	037-963	CAPACITOR, TANT., 33 uF, 10V	C3	1	1	1	1	1
7	064-116	CAPACITOR, CER., .01 uF, 50V	C2,4	2	2	2	2	2
8								
9								
10	581-475	DIODE, LIGHT EMITTING, AMBER	DS4	1	1	1	1	1
11	581-647	LED ARRAY, 4 ELEMENT	DS1,2,3	3	3	3	3	3
12	135-159	HEADER ASSEMBLY, 6 POS., RIGHT ANGLE	CP J5	1	1	1	1	1
13	135-025	HEADER ASSEMBLY, 28 PIN	CP J3	1	1	1	1	1
14								
15	586-759	INTEGRATED CIRCUIT, 7408	A11	1	1	1	1	1
16	586-890	INTEGRATED CIRCUIT, 7417	A12,13	2	2	2	2	2
17	586-450	INTEGRATED CIRCUIT, 74164	A2	1	1	1	1	1
18	587-537	INTEGRATED CIRCUIT, 74LS221	A1	1	1	1	1	1
19	586-753	INTEGRATED CIRCUIT, 75451B	A14	1	1	1	1	1
20	581-525	INTEGRATED CIRCUIT, READOUT	A3-10	8	8	8	8	8
21								
22	066-821	RESISTOR, C.F., 820 OHMS, 1/4W, 5%	R4,8,9,10	4	4	4	4	4
23	066-666	RESISTOR, C.F., 2.7K OHMS, 1/4W, 5%	R1	1	—	1	—	—
24	066-816	RESISTOR, C.F., 390 OHMS, 1/4W, 5%	R2	1	1	1	1	1
25	066-840	RESISTOR, C.F., 680 OHMS, 1/4W, 5%	R3	1	1	1	1	1
26	066-812	RESISTOR, C.F., 100 OHMS, 1/4W, 5%	R5,6,7	3	3	3	3	3
27	066-720	RESISTOR, C.F., 3.3K OHMS, 1/4W, 5%	R1		1	—	—	—
28	066-689	RESISTOR, C.F., 2.2K OHMS, 1/4W, 5%	R1				1	1
29	120-940	SWITCH, PUSHBUTTON SPDT	S1-4	4	4	4	4	4
30	121-219	SWITCH, PUSHBUTTON, WHITE	REF: S2-4	3	3	3	3	3
31	121-322	SWITCH, PUSHBUTTON, RED	S1	1	1	1	1	1
32	615-004	WIRE, BARE, 24 AWG	REF: S1-4	A/R	A/R	A/R	A/R	A/R
33	600-232	SLEEVING, TEFLON, 24 AWG	REF: S1-4	A/R	A/R	A/R	A/R	A/R



Assembly No. 1400420. Time Readout PWA

DISTR CODE: S



NOTES: UNLESS OTHERWISE SPECIFIED –

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%;
2. CAPACITANCE VALUES ARE IN MICROFARADS, 50V.
3. JUMPER E5 TO E6 FOR SIMULTANEOUS LOCAL/REMOTE CONTROL.
4. THIS SCHEMATIC REFLECTS PWA 1400420-05

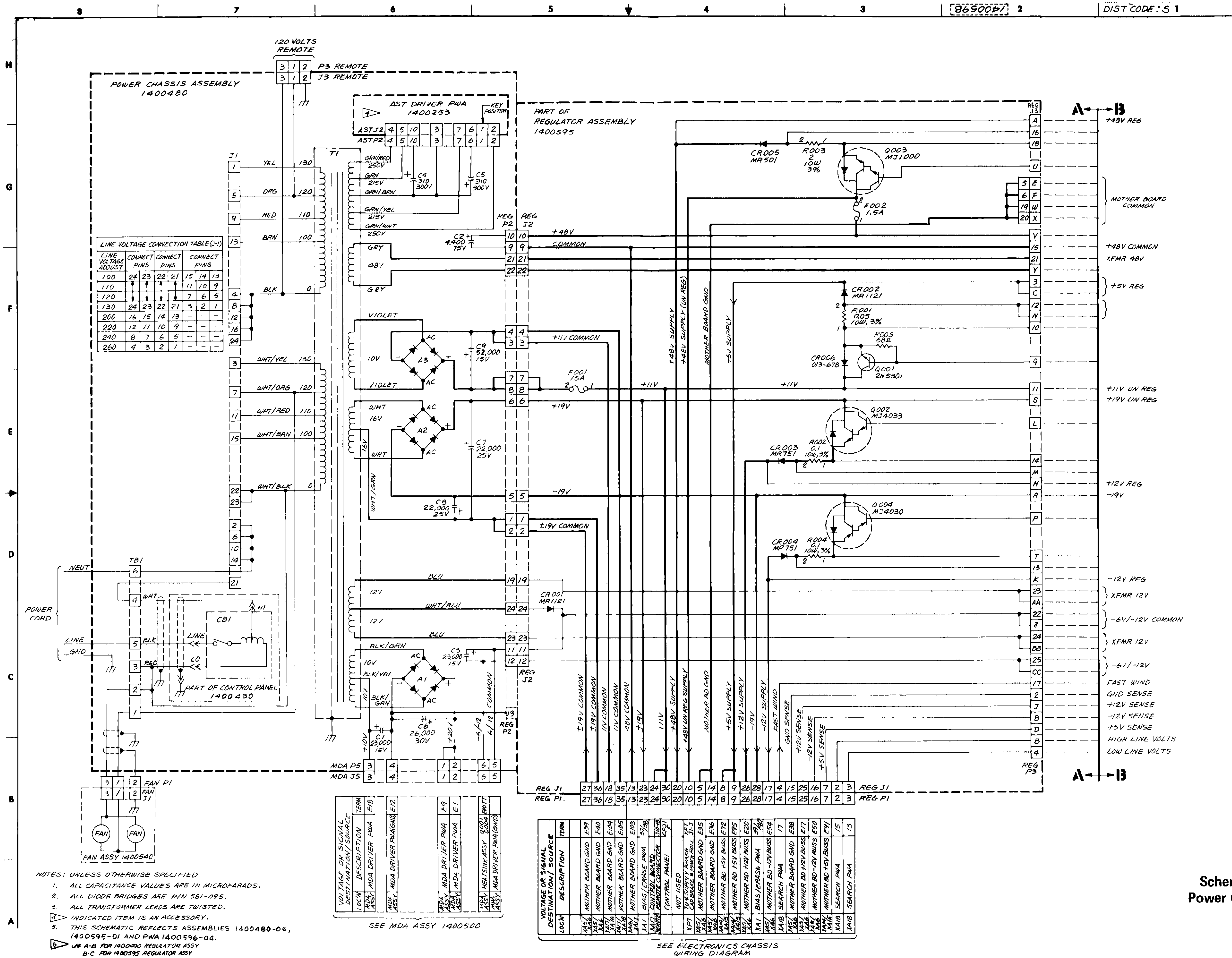
REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A14	
C4	
CPJ5	CPJ1,2,4
DS4	
E11	
FL1	
R10	
S4	

I. C. LIST

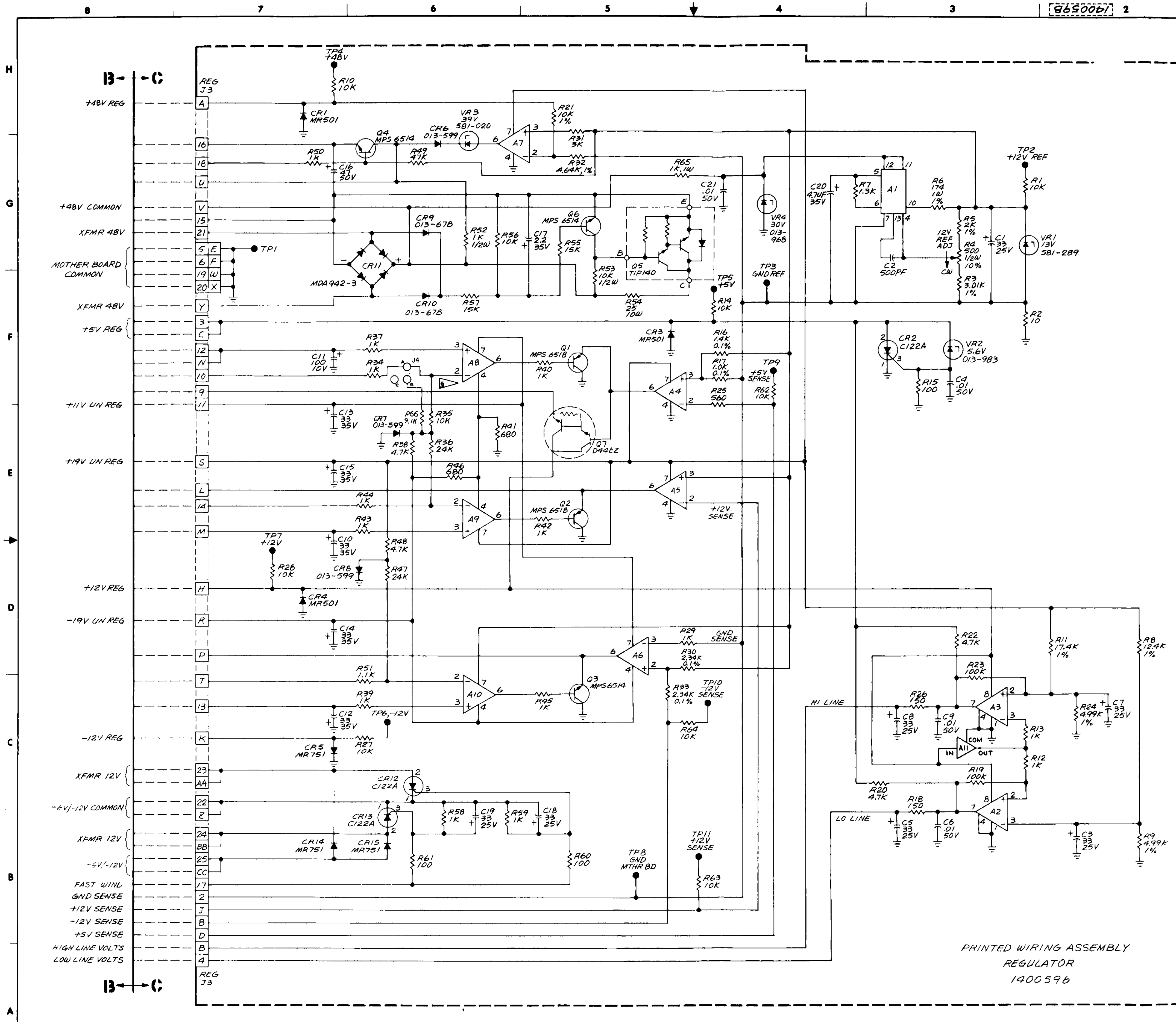
REFERENCE DESIGNATION	A1	A2	A3,4,5,6 7,8,9,10	A11	A12,13	A14
AMPEX P/N	587-537	586-450	581-525	586-759	586-890	586-753
VENDOR P/N	SN74LS221	SN74164	5082-7340	SN7408N	SN7417	SN75451B
VOLTAGE (PIN)	+5V (16)	+5V (14)	+5V (7)	+5V (14)	+5V (14)	+5V (8)
GROUND PIN	8	7	6	7	7	4

Schematic No. 1400422D.
Time Readout

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01
1				
2				
3	1400598	SCHEMATIC PWR CHASSIS & REGULATOR ASSEMBLY		REF
4				
5				
6	013-678	DIODE, POWER CD451	CR 006	1
7				
8	059-408	RESISTOR, POWER, 0.05 OHM, 10W, 3%	R001	1
9	066-677	RESISTOR, C.F., 68 OHMS, 1/4W,5%	R005	1
10	066-830	RESISTOR, C.F., 10K, 1/4W,5%	R35	1
11				
12				
13	070-431	FUSE, 15 AMP,FAST BLOW	F001	1
14				
15	261-024	EYELET		3
16				
17	471-061	SCREW, PAN HD, 4-40 X 5/16 LG.		1
18	492-008	NUT, HEX, 4/40		1
19	501-976	WASHER, SHOULDER, NYLON		
20				
21	580-244	TRANSISTOR, SILICON,(2N5301)	Q001	1
22	580-830	TRANSISTOR, SILICON,(D44E2)	Q7	1
23				
24	580-648	INSULATOR, TRANSISTOR, MICA REF:	Q7	1
25				
26				
27	615-095	WIRE, SOLID, INSULATED, 26 AWG		24''



Schematic No. 1400598G.
Power Chassis and Regulator
(Sheet 1 of 2)



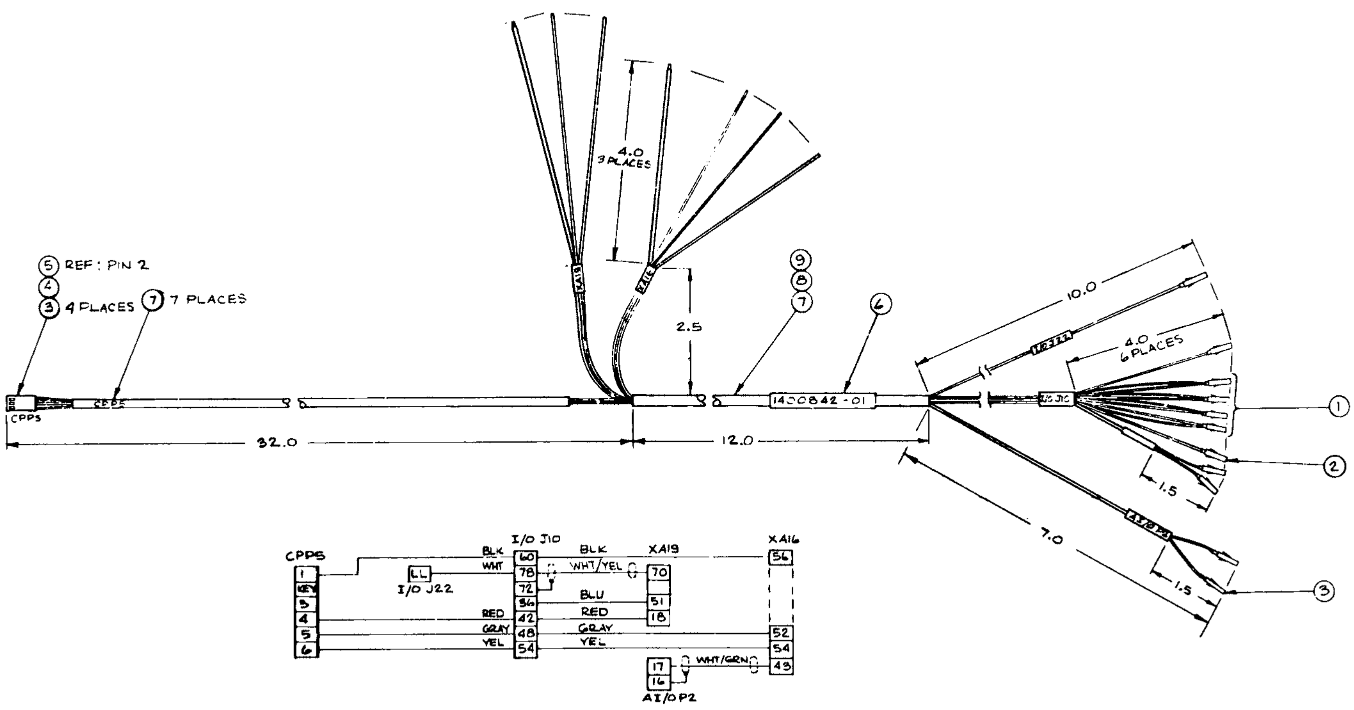
FIELD SERVICE COMPONENT SUBSTITUTION LIST	
AMPEX P/N	NEAREST COMM. EQUI.
013-599	IN4153
013-600	MDA 942-3
013-678	IN4005
013-871	IN4006
013-968	IN4751A
013-983	IN752A
581-020	IN4754A
581-289	IN4743A

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
A11	
C21	
CR15	
CR006	
F002	
J4	
Q7	
Q004	
R66	
R005	
VR4	
TP11	

I. C. LIST			
REF DES	A1	A2,3	A4,5,6,7,8,9,10
AMPEX P/N	586-449	587-891	586-764
VENDOR P/N	UA723HC	UA311TC	UA741TC
VOLTAGE (PIN)			
GROUND PIN			
REF DES	A11		
AMPEX P/N	587-771		
VENDOR P/N	78L05		
VOLTAGE (PIN)	—		
GROUND PIN	—		

Schematic No. 1400598G.
Power Chassis and Regulator
(Sheet 2 of 2)

01	ITEM NO.	PART NUMBER	DESCRIPTION
A/R	9		CABLE, SHIELDED, 1 COND, 24 GA.
A/R	8		WIRE, STRANDED, 24 GA.
A/R	7		SLEEVING, FLEXIBLE
A/R	6		SLEEVING, SHRINKABLE
1	5	167-854	CONNECTOR PART, KEY REF: CPP5-2
1	4	167-670	HOUSING, PLUG, 6 POS
6	3	167-129	CONTACT, SOC. 22-26 GA.
5	2	166-224	CONTACT, SOC. 24-26 GA.
4	1	166-199	CONTACT, SOC. 20-22 GA.



Assembly No. 1400842. Time Code Reader/Generator Modification Cable

1400859-01 TIME CODE READER/GENERATOR KIT (VPR-2 SERIAL NOS. 400-1849 REV. D

1	1400163-04	PWA, T.C. READER/GENERATOR	1								
2											
3	1400513-07	LABEL, P.W.A. LOCATION	1								
4	1400599-01	KIT, POWER SUPPLY UPGRADE ▷1	1								
5	1809449	T.C. READER/GENERATOR ACCESSORY MANUAL OPERATIONS AND	1								
6		MAINTENANCE									
7	1809457	INSTALLATION INSTRUCTIONS	1								
8	1809473	POCKET INSTRUCTIONS	1								

NOTE:

▷1 NOT NEEDED AFTER SERIAL NO. 1850

1400860-03 TIME CODE READER/GENERATOR KIT (VPR-2 SERIAL NOS. 1850 AND UP AND ALL VPR-2B'S) REV. U

ITEM NO.	PART NUMBER	DESCRIPTION	REF DESIG	QTY REQD PER DASH NUMBER -01	-02	-03
1	1400160-10	PWA, T.C. READER/GENERATOR				-
2	1400163-01	PWA, T.C. READER/GENERATOR				-
3	1400513-07	LABEL, DOOR				1
4						
5	1809449	T.C. READER/GENERATOR ACCESSORY MANUAL OPERATION				1
6		AND MAINTANENCE				
7	1809457	INSTALLATION INSTRUCTIONS				1
8	1809473	POCKET INSTRUCTIONS				1
9						
10	1400163-04	PWA, T.C. READER/GENERATOR				1

AMPEX

AUDIO-VIDEO
SYSTEMS DIVISION

CATALOG NO. 1809449-03
ISSUED: APRIL 1981